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Development, Demonstration, and Device Physics of FET-Accessed One-Transistor GaAs Dynamic Memory Technologies

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LIST OF SYMBOLS

α	Semiconductor Bandgap Temperature Coefficient
A	Area
A*	Effective Richardson Constant
A_{Cap}	Storage Capacitor Area
A_{Gate}	FET Gate Diode Area
C	Capacitance
C_J	Junction Capacitance
C_{J0}	Zero-Bias Junction Capacitance
c_{ns}	Surface Electron Capture Coefficient ($cm^3\ sec^{-1}$)
c_{ps}	Surface Hole Capture Coefficient ($cm^3\ sec^{-1}$)
C_{PNP}	PNP Device Capacitance
$C_{PNPNorm}$	Normallized PNP Device Capacitance
C_{PNP0}	Zero-Charge PNP Device Capacitance
$C_{PNP}(0)$	Charged PNP Device Capacitance at $t = 0^+$
$D_{IT}(E)$	Surface State Density ($\#/cm^2\text{-}eV^{-1}$)
ΔE	Frenkel Barrier Lowering Parameter
$\Delta\phi$	Schottky Barrier Image Force Correction
ΔV_{off}	Voltage Below Threshold to Totally Turn-Off FET
ΔV_{on}	Voltage Above Threshold to Sufficiently Turn-On FET
e	2.718282
E_C	Conduction Band Minimum
E_G	Semiconductor Bandgap
E_{GE0}	Extrapolated Zero-Temperature Bandgap
E_i	Intrinsic Fermi Level
ε	Electric Field
ε_{Peak}	Peak PN Junction Electric Field

ε'_{Peak}	Peak PiN Junction Electric Field
ε_S	Semiconductor Dielectric Constant
E_T	R-G Energy Level
E_T'	R-G Center Energy Level Adjusted For Degeneracy
E_V	Valence Band Maximum
F_N	Electron Quasi-Fermi Level
F_P	Hole Quasi-Fermi Level
ϕ	Electrostatic Potential
ϕ_b	Potential Barrier Height
ϕ_{bn}	Schottky Barrier Height
G_B	Bulk Generation Rate ($cm^{-3}sec^{-1}$)
G_P	Perimeter Generation Rate ($cm^{-2}sec^{-1}$)
I	Current
I_{BG}	Current Due to Bulk Generation
I_{Cap}	Storage Capacitor Leakage Current
I_D	Transistor Drain Current
I_{DMin}	Transistor Drain Current Minimum
I_{DS}	Drain-to-Source Current
I_{DSub}	Drain-to-Substrate Current
I_{DSSub0}	Drain-to-Source Current at $V_G = V_T$
I_{GS}	Gate-to-Source Current
I_{PG}	Current Due To Perimeter Generation
I_R	Reverse Leakage Current
I_{RPN}	PN Junction Reverse Leakage Current
I_{RSB}	Schottky Barrier Reverse Leakage Current
I_{Tran}	DRAM Cell Transistor Leakage Current
I_{SD}	Source-to-Drain Current
I_{SG}	Gate-to-Drain Current
J	Current Density (current/area)
J_{ACap}	Area-Scaled DRAM Capacitor Leakage Current Density
J_{AGate}	Area-Scaled FET Gate Diode Leakage Current Density
J_{BG}	Current Density Due To Bulk Generation
J_{Meas}	Measured Current Density
J_{PCap}	Perimeter-Scaled DRAM Capacitor Leakage Density

J_{PGate}	Perimeter-Scaled FET Gate Diode Leakage Density
J_{PG}	Current Density Due To Perimeter Generation
J_S	Schottky Barrier Saturation Current Density
J_R	Reverse Leakage Current Density
k	Boltzmann Constant
κ	Short-Channel Threshold Shift Coefficient
K_{GC}	DRAM Cell Gate Width to Capacitor Width Ratio
L_{Cap}	DRAM Storage Capacitor Length
L_{Gate}	FET Gate Length
n	Electron Concentration
n_{Sub}	Subthreshold Ideality Factor
N_A	Acceptor Impurity Concentration (#/cm^3)
N_{ATop}	Top P-Layer Doping in PNP Capacitor
$N_{ABottom}$	Bottom P-Layer Dopeing in PNP Capacitor
N_C	Conduction Band Effective Density of States
N_D	Donor Impurity Concentration (#/cm^3)
n_i	Intrinsic Carrier Concentration (#/cm^3)
n_{Sub}	Drain-to-Source Subthreshold Ideality Factor
N_V	Valence Band Effective Density of States
p	Hole Concentration
P	Perimeter
P/A	Perimeter to Area Ratio
P_{Cap}	Storage Capacitor Perimeter
P_{Gate}	FET Gate Diode Perimeter
π	Pi
q	Electron Charge
Q	Total Charge
Q(0), Q(t=0$^+$)	Initial Charge at t=0
Q(t)	Charge at Time t
$Q_{Norm}(t)$	Normallized Charge at Time t
Q_{SB}	Schottky Barrier Junction Charge
ρ_{Cap}	DRAM Capacitor Charge Density
s_o	Surface Generation-Recombination Velocity
S_{Sub}	Drain-to-Source Subthreshold Current Slope

t	Time
T	Temperature
τ_C	Capacitance Transient Time Constant
τ_n	Electron Generation Lifetime
τ_p	Hole Generation Lifetime
τ_{nB}	Bulk Electron Generation Lifetime
τ_{pB}	Bulk Hole Generation Lifetime
τ_S	1/e Storage Time
τ_{SCap}	DRAM Capacitor 1/e Storage Time
τ_{SCell}	DRAM Cell 1/e Storage Time
V	Voltage
V_A	Applied Voltage
V_{bi}	Built-In Diode Junction Voltage
V_{DS}	Drain-to-Source Voltage
V_G	Transistor Gate Voltage
$V_G(I_{DMin})$	Gate Voltage at Drain Current Minimum
V_{GM}	Maximum GaAs FET Positive Gate Voltage
V_{high}	Logic High (One) Voltage
V_i	PiN Junction i-Layer Voltage Drop
V_{low}	Logic Low (Zero) Voltage
V_{NM}	Worldine Off Noise Margin Voltage
V_R	Reverse Bias Voltage
V_{SB}	FET Source Bias Voltage
V_{Subs}	Substrate Voltage
V_T	Threshold Voltage
V_{T0}	Zero-Drain Bias Threshold Voltage
$V_{WL(off)}$	Wordline Voltage to Turn-Off DRAM Access FET
$V_{WL(on)}$	Wordline Voltage to Turn-On DRAM Access FET
V_{Write}	Capacitor Write Pulse Voltage
W	Depletion Width
W'	PiN Junction Depletin Width
W_{Cap}	DRAM Capacitor Width
W_G	Generation Width
W_{Gate}	FET Gate Width

W_{PN}	PN Junction Depletion Width
W_{PN0}	PN Junction Depletion Width at Zero Bias
W_{SB}	Schottky Junction Depletion Width
W_{SB0}	Schottky Junction Depletion Width at Zero Bias
W_0	Zero-Bias Equilibrium Depletion Width
W'_0	PiN Junction Zero-Bias Equilibrium Depletion Width
x	Position
x_i	Undoped i-Layer Thickness
x_N	Position of Edge of Depletion Region in N Material
x_P	Position of Edge of Depletion Region in P Material

LIST OF ACRONYMS

ALE	Atomic Layer Epitaxy
AND	AND Logic Function
CMOS	Complementary Metal-Oxide-Semiconductor
DAS	Digital Analysis System
DCAM	Dynamic Content Addressable Memory
DRAM	Dynamic Random Access Memory
D-MESFET	Depletion-Mode MESFET
ECL	Emitter Coupled Logic
ehp	Electron-hole pairs
E-MESFET	Enhancement-Mode MESFET
eV	Electron-Volt
FET	Field Effect Transistor
HBT	Heterojunction Bipolar Transistor
HIGFET	Heterojunction Insulated Gate Field Effect Transistor
IC	Integrated Circuit
I/O	Input/Output
JFET	Junction Field Effect Transtor
Kb	Kilobit = 1,000 bits
LSI	Large Scale Integration
Mb	Megabit = 1,000,000 bits
MBE	Molecular Beam Epitaxy
MESFET	Metal-Semiconductor Field Effect Transistor
MIM	Metal-Insulator-Metal
MIM-C	Metal-Insulator-Metal Capacitor
MIPS	Million Instructions Per Second
MOCVD	Metal-Organic Chemical Vapor Deposition
MODFET	Modulation Doped Field Effect Transistor

MOS	Metal-Oxide-Semiconductor
MOS-C	Metal-Oxide-Semiconductor Capacitor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
OR	OR Logic Function
R-G	Recombination-Generation
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
SRAM	Static Random Access Memory
VLSI	Very Large Scale Integration
XNOR	Exclusive Not OR Logic Function
XOR	Exclusive OR Logic Function
1-T DRAM	One-Transistor Dynamic Random Access Memory

ABSTRACT

The introduction of digital GaAs into modern high-speed computing systems has led to an increasing demand for high-density memory in these GaAs technologies. To date, most of the memory development efforts in GaAs have been directed toward four- and six-transistor static RAM's, which consume substantial chip area and dissipate much static power resulting in limited single-chip GaAs storage capacities. As it has successfully done in silicon, a one-transistor dynamic RAM approach could alleviate these problems making higher density GaAs memories possible. This dissertation discusses theoretical and experimental work that presents the possibility for a high-speed, low-power, one-transistor dynamic RAM technolgy in GaAs.

The two elements of the DRAM cell, namely the charge storage capacitor and the access field-effect transisotor have been studied in detail. Isolated diode junction charge storage capacitors have demonstrated 30 minutes of storage time at room temperature with charge densities comparable to those obtained in planar silicon DRAM capacitors. GaAs JFET and MESFET technologies have been studied, and with careful device design and choice of proper operating voltages experimental results show that both can function as acceptable access transistors. One-transisor MESFET- and JFET-accessed DRAM cells have been fabricated and operated at room temperature and above with a standby power dissipation that is only a small fraction of the power dissipated by the best commercial GaAs static RAM cells. A 2 x 2 bit demonstration array was built and successfully operated at room temperature to demonstrate the addressable read/write capability of this new technology.

CHAPTER 1 - INTRODUCTION

1.0 The Emergence of LSI Digital GaAs

Since the beginning of the semiconductor age, silicon has been the material of choice in the manufacture of solid state integrated circuits. It has proven to be a well-developed reliable technology suitable for most of today's integrated circuit applications. In recent years there has been an increasing demand for extremely high speed circuits for use in several specialized areas. Fundamental physical limitations inherent to silicon have prevented it from meeting the stringent requirements of leading microwave, supercomputing, and optical technologies.

Gallium Arsenide (GaAs) is a compound semiconductor that is better suited for ultra high-speed applications than silicon thanks to higher free electron mobilities. Unfortunately GaAs has some undesirable properties which to date have kept it from becoming a widely used material, even in high speed applications. Perhaps the largest obstacle to gallium arsenide's development has been its poor electrochemical surface characteristics. High quality insulating dielectric material cannot be grown or deposited on GaAs without forming an unacceptably high density of electrical defects at the semiconductor surface [15,26,27]. These defects to date have prevented the development of a true GaAs analog to the Si-SiO_2 MOSFET (Metal Oxide Semiconductor Field Effect Transistor), the workhorse transistor of the computer chip revolution.

The absence of a true insulated gate FET technology has seriously hindered the development of large scale GaAs integrated circuits. It is only recently that alternative technologies have overcome considerable processing and circuit design obstacles to achieve Very Large Scale Integration (VLSI) in GaAs. GaAs digital integrated circuits based on

Junction Field Effect Transistors (JFET's) and MEtal Semiconductor Field Effect Transistors (MESFET's) are infiltrating the high speed digital marketplace [44-51]. The Cray III supercomputer is implemented in GaAs MESFET technology, and other companies like Gigabit, Vitesse, and TriQuint are marketing digital GaAs products used in demanding high speed computing environments. McDonnell Douglas has produced a modest 64 MIPS GaAs JFET RISC microprocessor, while Texas Instruments has successfully developed its own microprocessor using bipolar GaAs Emitter Coupled Logic (ECL).

1.1 The Need of Higher Density GaAs RAM

Although significant progress has been made, further technological improvements are necessary if digital GaAs IC's are to offer competitive performance advantages over their silicon counterparts. This is particularly evident in the area of high-speed memory chips which are used as cache RAM's in ultra-fast computing systems. Figure 1.1 shows a survey of high-speed RAM chips reported from 1985 through 1990 in the form of an access speed versus single-chip storage capacity graph. Although low capacity ($\leq$ 16 Kb) GaAs SRAM chips compete well with their silicon counterparts, there is a glaring absence of large capacity GaAs memory chips.

This absence is a serious obstacle to the development of high-speed GaAs computing systems. Computational system performance is enhanced by maximizing both the size and speed of cache RAM. Inter-chip propagation delays and cost considerations make it advantageous to minimize the number of chips in a system cache RAM, and most modern microprocessors now include substantial amounts of on-chip cache RAM. If GaAs based computing systems are to take full advantage of on-chip cache RAM architecture, it is clear that higher density GaAs memories must be developed.

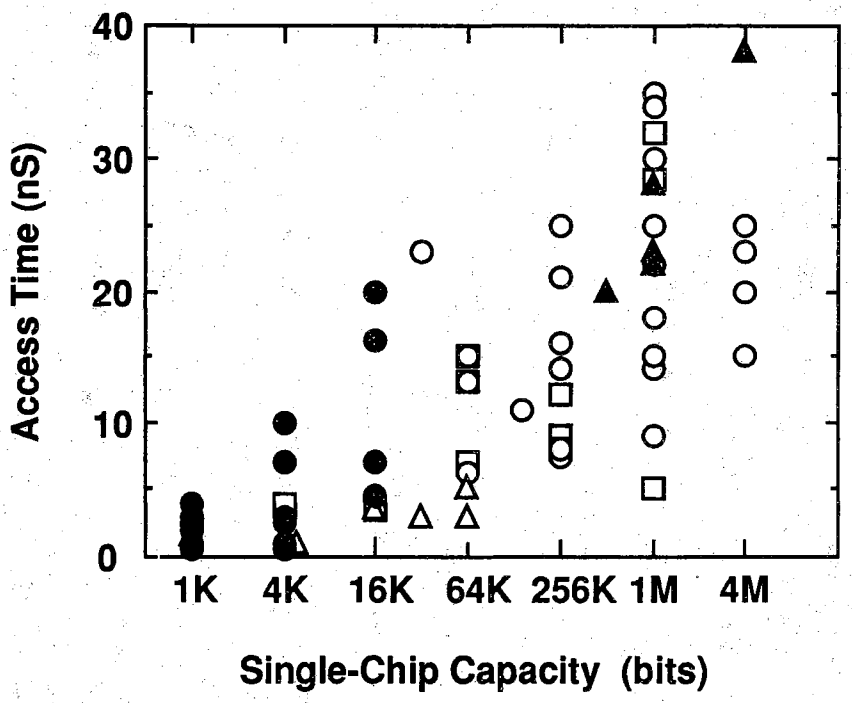


Figure 1.1 High speed RAM's reported from 1985 through 1990. Note that GaAs RAM chip sizes do not exceed 16 Kb. This data was accumulated from References [44-50], [63-67], and [69-94].

1.2 Current State of GaAs Memory - The SRAM Cell

An analysis of present-day GaAs memories reveals not only the reasons for their limited storage capacities, but also some of the difficulties in processing and circuit design that has hindered the widespread development of digital GaAs IC's. The basic storage element of GaAs digital memory is the Static Random Access Memory (SRAM) cell shown in Figure 1.2. From a circuits point of view the cell is nothing more than a pair of cross coupled inverters isolated from the bitlines by access transistors [57]. Positive feedback between the opposite-state inverters maintains the logic state during storage. Reading and writing is accomplished by turning on the access transistors with the wordline and appropriately sensing or driving the bitlines.

When implemented in state of the art GaAs JFET or MESFET technology, the SRAM cell is too large and dissipates too much power to allow the practical fabrication of large memory arrays. This fact is evidenced by Table 1.1, which surveys the performance of GaAs SRAM's reported at the 1988 IEEE GaAs IC Symposium. In addition to the yield difficulties large die sizes produce, the intrachip propagation delays hamper overall circuit perfomance. The area problem arises from the fact that at least four properly isolated transistors are needed for each bit. In standard LSI planar ion implanted FET processes the minimum distance between two adjacent FET's in GaAs is dictated by parasitic backgating instead of minimum patterned feature sizes [37,38,40]. Gains made in shrinking individual device areas translate into smaller improvements in overall SRAM cell area.

The power problem is due to the fact that significant current is always being drawn by one of the cross-coupled inverters of the SRAM, and that GaAs FET's are operated in overdrive mode for increased speed [43]. Complementary logic analogous to silicon CMOS could greatly reduce the power dissipation problem by cutting-off current flow through the inverters in an idle state [68]. This approach has not proven feasible however because GaAs hole mobilities are too low to make reasonably sized high-speed (i.e., high-current) p-channel FET's [109].

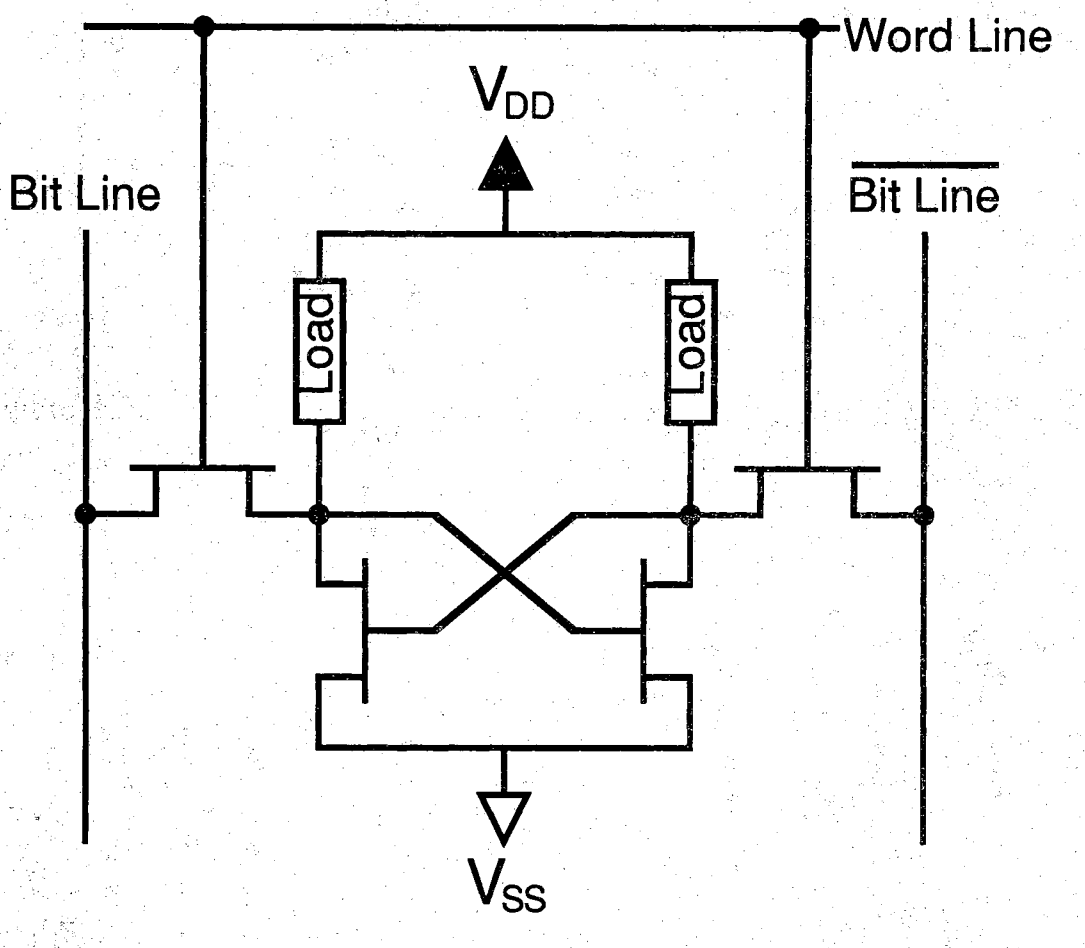


Figure 1.2 Circuit diagram of a Static Random Access Memory (SRAM) cell.

Table 1.1 Survey of high-speed GaAs SRAM's reported at the 1988 GaAs IC Symposium.

SRAM Chip	Cell Size (μm^2)	Die Size (mm^2)	Chip Power	Access Time
Vitesse 1Kb MESFET [48]	31 x 21	2.0 x 1.7	0.6 W	2.5 ns
Gigabit 4Kb MESFET [44]	40 x 35	4.2 x 3.9	1.9 W	3 ns
Mitsubishi 4Kb MESFET [45]	35 x 29	4.8 x 4.6	0.85 W	7 ns
McD. D. 16Kb JFET [47]	49 x 32	8.2 x 5.6	0.68 W	16 ns

1.3 The DRAM Concept for High Density Memories

In contrast to the limited storage capacity of GaAs SRAM chips, Dynamic Random Access Memories (DRAM's) manufactured in silicon are widely available in sizes of 1 and 4 megabits (Mb) per chip. 16 and 64 Mb DRAM chips have been reported, and designs for 256 Mb chips are being researched [59,60,110-113]. Although DRAM's have somewhat slower access times than SRAM's, their immense storage capacities and low power dissipation have made them a predominant memory technology of the computer revolution. The basic storage element of the DRAM is shown in Figure 1.3. It consists of a charge storage capacitor connected to the bitline through an access transistor.

Stored data is represented by charge stored on the capacitor, and access to the bitline for reading and writing is controlled by the transistor [57]. In many DRAM designs the presence of a charge on the capacitor represents a logic one, while a neutral charge represents a stored zero. In the idle storage state the access transistor is turned off so that the capacitor and bitline are completely isolated from each other. To write the cell the bitline is set to either the logic 1 or logic 0 voltage, and the access transistor is turned on by the wordline. The connection through the turned-on transistor forces the voltage on the capacitor to be nearly equal to the bitline voltage, and the capacitor remains charged when the access transistor is turned off.

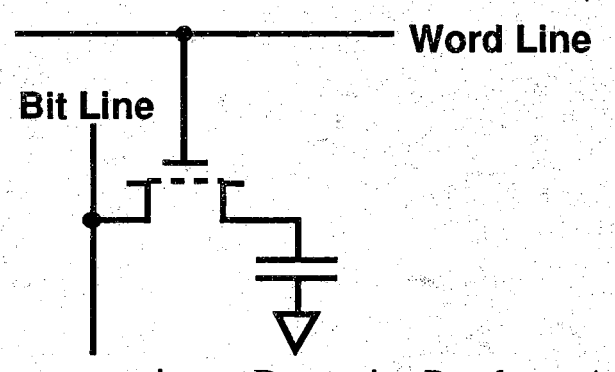


Figure 1.3 The one-transistor Dynamic Random Access Memory (DRAM) cell.

Reading the 1-T DRAM cell focuses on determining the presence of stored charge. In contrast to the write operation where the bitline is set to a specific voltage, the bitline voltage is permitted to change during a read operation. The cell is addressed by turning on the access transistor with the wordline, and charge sharing between the storage capacitor and the bitline causes the potential of the bitline to change depending on the stored data. Though small, the change in bitline voltage is detected by a sense amplifier located at the end of the bitline, and a corresponding one or zero is passed on to the memory output circuitry. Because most of the charge in the capacitor is lost to the bitline through charge sharing, the data that was read must immediately be written back to the cell [57].

The one-transistor memory cell is considered "dynamic" because the stored data needs to be periodically refreshed as charge leaks from the capacitor over time. Refreshing is accomplished by simply reading and writing back the contents of each memory location at regular intervals. If parasitic leakage mechanisms are large enough that cell storage times are too short, the DRAM chip will spend an inefficient amount of time conducting refreshes instead of storing and retrieving useful data. With refresh rates on the order of 100 Hz and read/write access times around 50 nS, typical silicon DRAM chips based on low-leakage MOSFET access transistors exercise storage time to access time ratios of well over 100,000.

Although the operation and design is inherently more complex than SRAM's, DRAM's offer a storage capacity gain that has made them the dominant semiconductor memory of the computer revolution. The large storage capacities obtainable in DRAM's are largely a result of novel small-area implementations of the basic transistor-capacitor storage element [59,60]. Because the access transistor is turned-off in the storage state, standby power dissipation is minute and is not a limiting factor in DRAM chip design.

1.4 Statement of Thesis - Realization of GaAs DRAM Cells

Given the multi-megabit storage capacities that have been achieved with silicon DRAM's, it stands to reason that much higher GaAs bit

densities might be possible if 1-transistor DRAM cells could be implemented in GaAs. Unfortunately DRAM's rely on very low-leakage capacitors and access transistors that prior to this work had only been implemented in silicon using the MOS technology that GaAs sorely lacks. This work was undertaken to develop and implement the first one-transistor dynamic RAM cells using the non-MOS technologies available to GaAs.

1.5 Thesis Overview

1.5.1 Storage Capacitors

As the 1-T DRAM cell consists of a storage capacitor and an access field-effect transistor, a substantial portion of this thesis deals with the development and device physics of these components. Chapter 2 presents the extensive theoretical and experimental work done on storage capacitors. The capacitor design goals, namely high charge storage density and long charge storage time, are discussed in detail, and several schemes for capacitor implementation are proposed. Most of Chapter 2 is devoted to the PN junction charge storage capacitor, in which reverse-biased diode junctions are used to store charge [1,10,11]. Though simple, GaAs PN and PiN junction capacitors demonstrate half-hour storage times at room temperature, and excellent planar charge storage densities are achievable [1,2,4]. These experiments provided valuable insight into the physical leakage mechanisms that govern DRAM cell storage time.

1.5.2 Access Transistors

As most LSI GaAs chips are implemented using JFET's or MESFET's, these technologies are a natural choice for DRAM cell access transistors. Prior to this work conventional wisdom was that DRAM cells implemented with GaAs FET's would be too leaky and demand an impractical dynamic refresh rate [42]. This work has experimentally

demonstrated otherwise [2,3]. Chapter 3 discusses the minimization of GaAs JFET and MESFET off currents through careful device design and choice of proper operating voltages. The physical mechanisms that govern doped-channel FET leakage are presented theoretically and experimentally, and performance limiting factors are identified. Among these are gate diode leakage, drain diode leakage, and short-channel effects. Methods for reducing critical leakages were investigated, including a novel MESFET processing technique that reduced off leakage currents by more than a factor of 100 [8,9]. The proper choice of transistor thresholds and operating voltages is crucial to DRAM cell performance, so electrical design criteria that maximize storage time and access speed while minimizing power dissipation are presented.

1.5.3 GaAs DRAM Cells

This chapter combines the storage capacitor and access transistor concepts presented in Chapters 2 and 3 into complete operational DRAM cells. The fabrication, characterization, and successful room-temperature operation of the first reported JFET- and MESFET-accessed DRAM cells is presented [2,3]. The cells were based on the experimental epitaxial PN junction capacitors and FET's presented previously, so their behavior is compared with the results of Chapters 2 and 3. Just as isolated capacitor storage times shrank with smaller device sizes, the storage times of complete DRAM cells will also decrease. This issue along with a variety of other GaAs DRAM cell design issues are discussed. Some GaAs DRAM cell designs are proposed, and the some of the circuit design challenges issues that would be faced in the realization of large GaAs DRAM arrays are addressed.

1.5.4 Demonstration of a 2 x 2 DCAM Array

Although isolated FET-accessed cells were presented in Chapter 4, a small array of cells was constructed to conclusively demonstrate that GaAs

DRAM cells can be individually addressed for reading and writing. Chapter 5 describes the development, fabrication, and testing of a 2 x 2 bit experimental dynamic content addressable memory (DCAM) array.

CHAPTER 2 - STORAGE CAPACITORS

2.0 Introduction

This chapter deals solely with storage capacitor technologies that could be used to implement practical GaAs DRAM cells. A variety of technologies are available. The selection of the best capacitor technology is based on an evaluation of specific performance criteria, the optimization of which will profoundly impact the end capabilities of the complete DRAM chip. Though straightforward, the two most important criteria as outlined below are storage time and charge storage density. These design goals provide a strong basis for comparison of the various potential DRAM storage capacitor implementations discussed in this chapter. Other capacitor design-performance criteria, such as temperature performance, can be viewed as spin-offs of the first two critical design goals.

2.0.1 Storage Time

The first critical capacitor design goal is maximization of storage time through the minimization of charge leakage mechanisms. The isolated capacitor storage time must be long enough that the overall DRAM chip can have an efficient refresh rate as discussed in Section 1.3. Given a capacitor with an initial charge at time t = 0, the storage time is defined in this work as the time it takes for the charge to decay to 36.8% (1/e) of its initial value. It should be noted that this definition of storage time does not correspond directly to the amount of time that a cell could operate between refreshes, because most DRAM schemes require over 95% of the initial charge to be present for a proper read operation to occur (Section 1.3).

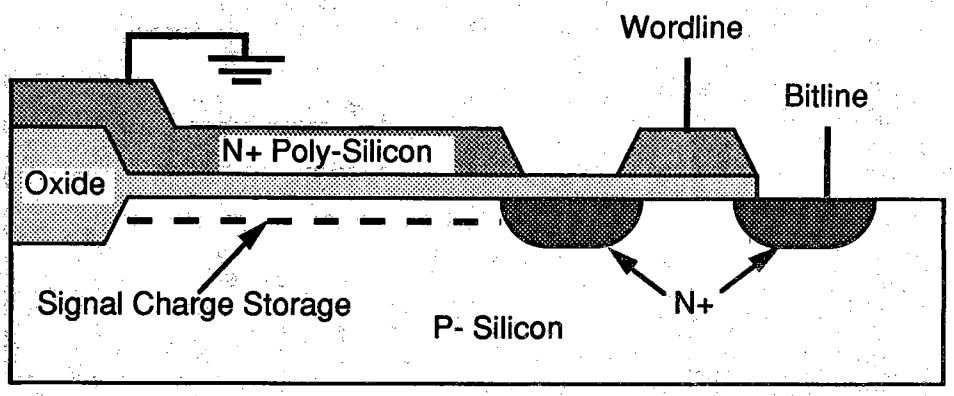
By dividing the measured 1/e storage time of a particular DRAM cell by 100, one can quickly calculate a reasonable estimate for the period of the refresh clock that would be required to operate a complete DRAM chip based on the given cell. As many silicon DRAM's operate with refresh clock rates in the range of 1 KHz, 1/e cell storage times on the order of 100 msec would prove satisfactory.

2.0.2 Charge Storage Density

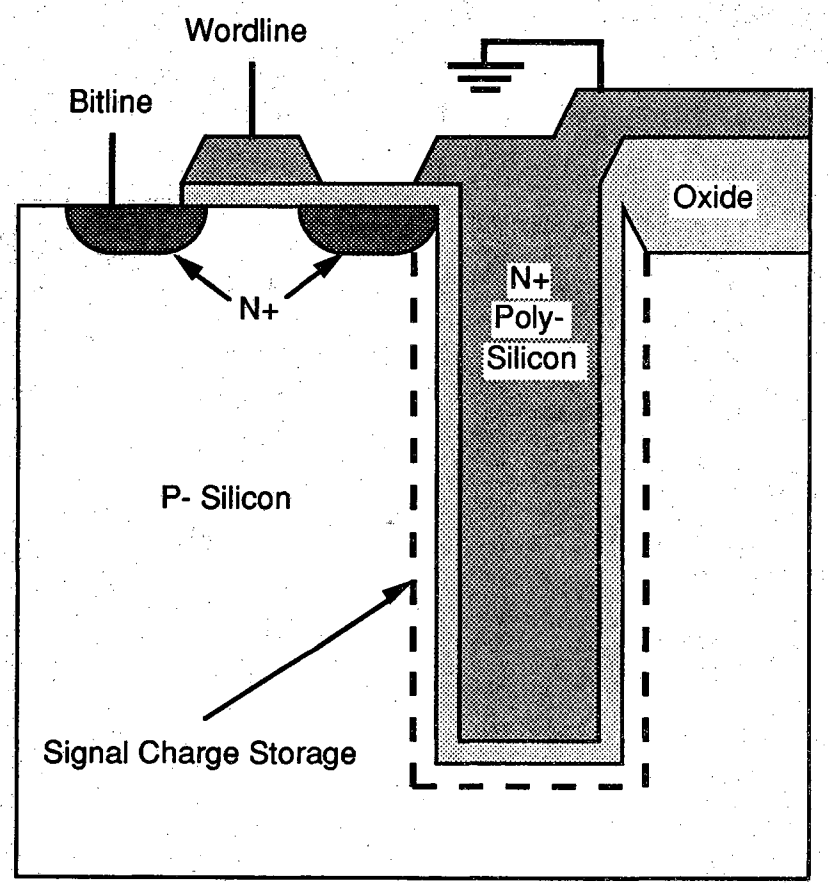
The second critical capacitor design goal is the maximization of stored charge per unit area, which is more commonly referred to as charge storage density. The criticality of this design goal cannot be understated, as largely it is improvements in this area that are driving silicon DRAM chips to 256 Mb and beyond. The amount of charge that needs to be stored in each individual DRAM cell is primarily determined by a variety of sense-amp circuit and noise error considerations (Chapter 4). By increasing the charge per unit area, the DRAM cell can be made smaller, and more data can be packed into the same chip area.

2.0.3 General DRAM Capacitor Structures

There are several general classes of electrical charge storage elements that can be used as DRAM capacitors. Most silicon DRAM's are implemented using metal-oxide-semiconductor (MOS) storage capacitors, where stored data is represented by the presence or absence of an inversion charge layer in the capacitor (Figure 2.1) [58,59,60]. The absence of a true GaAs MOS technology excludes the MOS storage capacitor class from consideration in this work. Defect states at the semiconductor-insulator interface dominate the electrical characteristics of GaAs MOS structures, prohibiting the formation of consistent charge layers near any GaAs surface [15,26,27,114].



a) Planar MOS DRAM cell



b) Trenched MOS DRAM cell

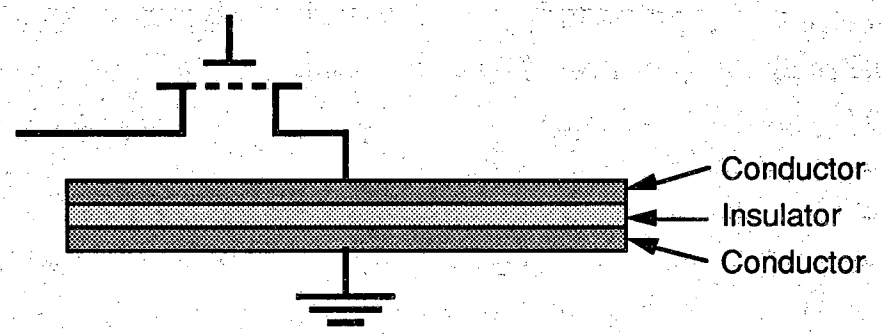
Figure 2.1. Silicon MOS DRAM cells. After Reference [59].

A second general class is the bona fide capacitor of Figure 2.2a, which consists of an insulating dielectric sandwiched by two conductive plates. Variations of this approach, some of which are quite exotic, are the storage elements of some state-of-the-art DRAM's (Figure 2.2b) [60]. The large amount of research being conducted elsewhere precluded the inclusion of experiments on true insulating dielectric capacitors in this work. Nevertheless it should not be overlooked that the insulating dielectric capacitor is a viable GaAs DRAM charge storage option.

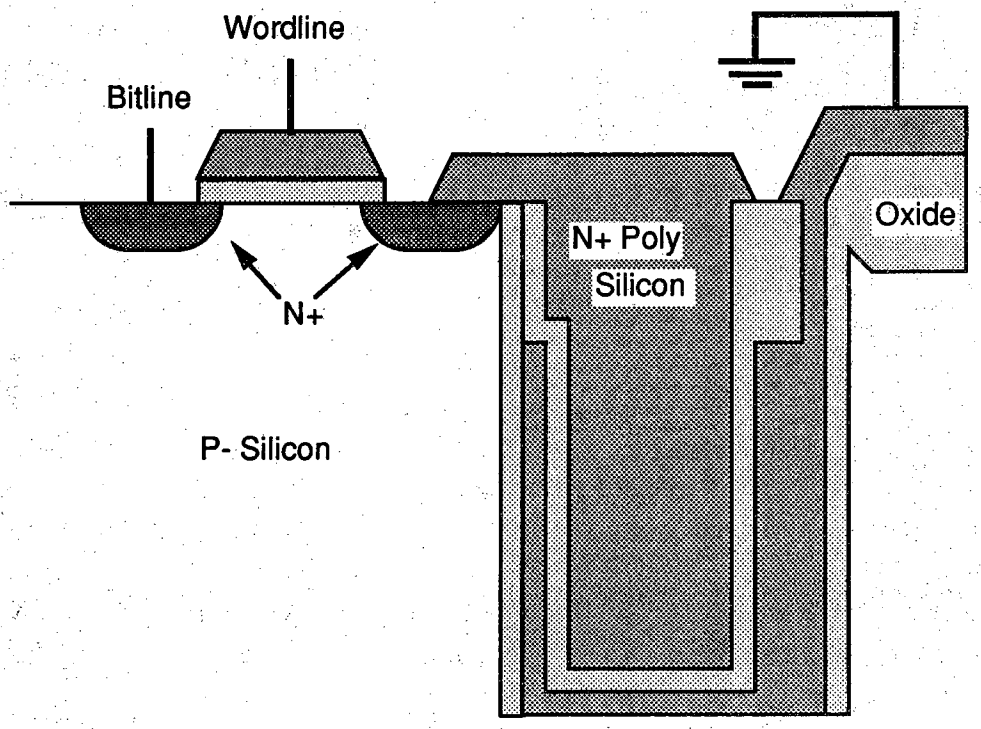
Extensive work at Purdue University has gone into the development of a third general class of charge storage element, in which isolated diode junctions are used to store charge [1-5,7,10-13]. This approach is particularly attractive because these diode junction capacitors are compatible with GaAs JFET and MESFET technologies already in widespread use. The research detailed throughout this chapter demonstrates that acceptable charge storage can be achieved in GaAs diode junction capacitors.

2.0.4 Chapter Outline

As it is a primary topic of research, most of this chapter deals with the general theory, development, and behavior of diode junction charge storage capacitors. Section 2.1 describes structure and measurement technique first used to demonstrate charge storage on PN junctions, the symmetric PNP capacitor. The charge stored on these capacitors decays with time through the reverse-biased leakage mechanisms described in Section 2.2. Using the results of the previous sections, analytical expressions for the stored charge as a function time are derived in Section 2.3, and key storage time issues are presented. Capacitor performance as a function of PN junction doping profile is discussed in Section 2.4, and it is concluded that performance generally improves with increased doping. Section 2.5 introduces the PiN junction capacitor, which improves the storage time of heavily-doped capacitors with very high charge storage densities.



a) Simple dielectric capacitor DRAM cell



b) Dielectrically insulated capacitor trench DRAM cell. After Ref. [59].

Figure 2.2 Pure dielectric capacitor DRAM structures.

Section 2.6 details experimental procedures, while Section 2.7 presents a vast array of experimental PNP results and compares them to the theories of previous sections. Section 2.8 describes experimental investigations into $Al_xGa_{1-x}As$ PiNiP devices which provided insight into fundamental physical leakage mechanisms that govern capacitor storage time. Section 2.9 documents an experimental effect whereby PNP capacitor storage times drop when large surface areas of the N-region are uncovered. In Section 2.10, a novel arsenic sulfide chemical treatment is applied to PNP capacitors to greatly reduce perimeter leakage and increase small-device storage times. Silicon DRAM's have turned to 3-D trenched capacitor structures to increase charge storage density, and the trenching technique could also be applied to PN junction storage capacitors. Section 2.11 outlines an experiment in which epitaxial growth of satisfactory PN junction diodes in and around etched trench sidewalls was accomplished for the first time [5,6].

Simple DRAM cell designs rely on non-symmetric P^+NP^- junction capacitors to accommedate undoped substrates, and Section 2.12 discusses the physical consequences of capacitors implemented on lightly doped substrates. Since most GaAs MESFET's and JFET's are implemented with ion-implanted technologies, Section 2.13 establishes the fact that acceptable low-leakage PN junctions have been achieved by ion-implantation. In the same manner that PN junctions can be used to store charge, metal-semiconductor Schottky diode junctions can also function as charge storage elements. Section 2.14 studies the feasibility of employing Schottky diodes as GaAs DRAM charge storage elements.

2.1 The PNP Charge Storage Capacitor

The concept of using PN junctions to store charge was demonstrated using the PNP capacitor structure shown in Figure 2.3. Unless explicitly stated otherwise, the dopings for the top and bottom P layers in any discussions of PNP capacitors in most of this chapter are always specified to be identical.

2.1.1 Writing Charge to the PNP Capacitor

With no charge stored in the capacitor, the middle N region is at ground and the PN junctions are in their zero bias equilibrium depletion widths (Figure 2.3a). Charge is written to the capacitor by applying a positive voltage to the right P contact (Figure 2.3b). This forward biases the right PN junction and reverse biases the left PN junction. Electrons flow out through the forward biased right junction and are not replenished by the reverse biased left junction. This pulls the N storage region to a positive potential. When the voltage applied to the top plate is suddenly restored to ground (Figure 2.3c), the potential of the N region will remain positive because there is no immediate source of carriers to replace the electrons that were extracted when applied voltage was positive. The positive N-region reverse-biases both PN junctions.

2.1.2 PNP Capacitor Charge

The charge Q stored on the capacitor is given by the number of majority carriers extracted from the sandwiched N-layer during a write pulse:

$$Q = 2qA\left(\frac{N_D N_A}{N_D + N_A}\right)(W - W_0) \tag{2.1}$$

where W_0 is the zero-bias equilibrium depletion width, W is the charged depletion width, and A is the device area. The factor of two accounts for the fact that there are two PN junctions in the PNP capacitor structure. The depletion widths are given by [52,56]:

$$W = \sqrt{\frac{2\varepsilon_S}{q}(V_{bi} + V_R)\left(\frac{N_A + N_D}{N_A N_D}\right)} \tag{2.2}$$

where V_R is the reverse-bias voltage across the PN junctions, and V_{bi} is the built-in junction potential given by:

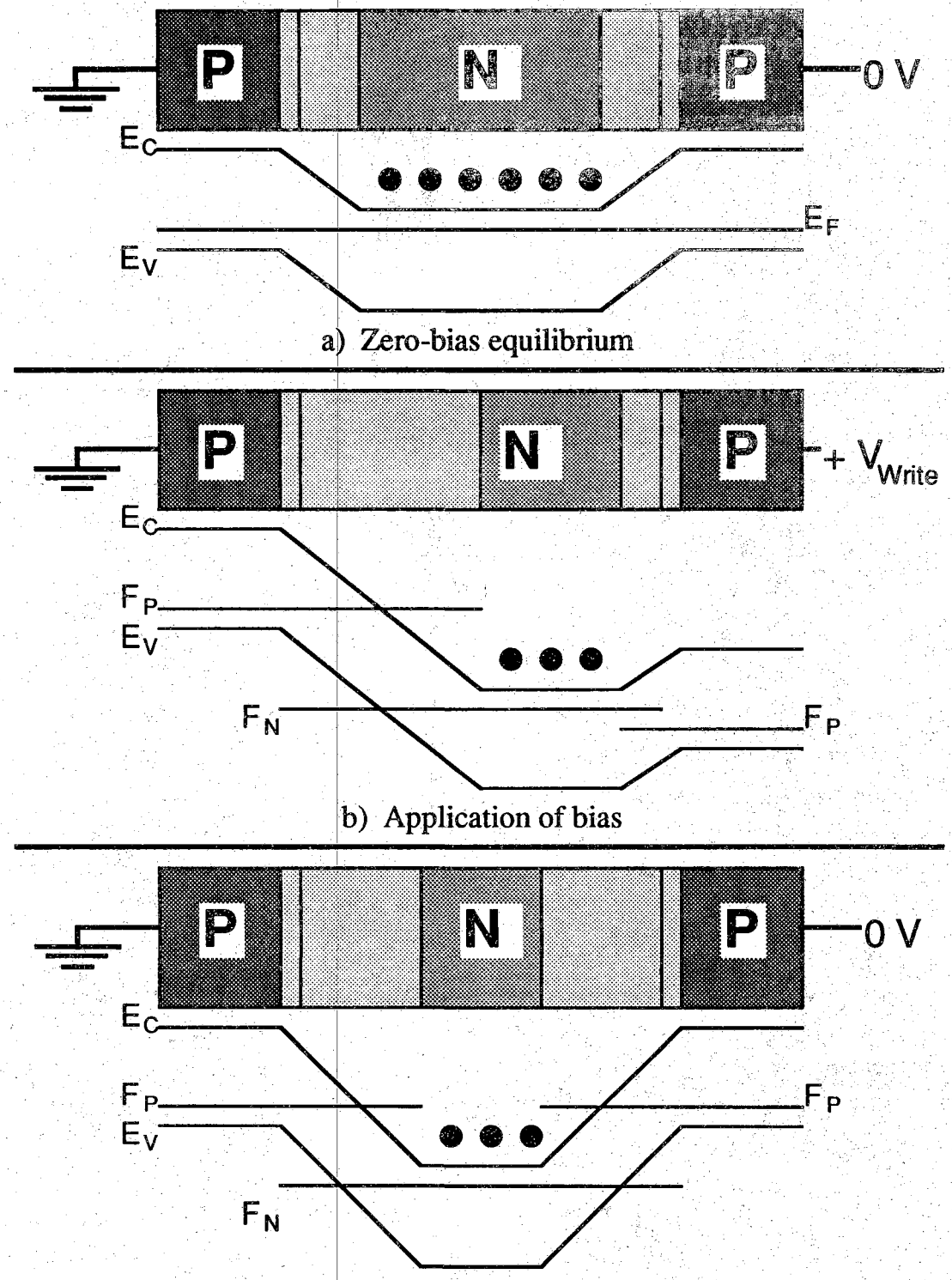


Figure 2.3 PNP capacitor and charge storage band diagrams.

$$V_{bi} = \frac{kT}{q} \ln\left[\frac{N_D N_A}{n_i^2}\right] \qquad (2.3)$$

for non-degenerate doping. Most of the experimental work presented in this report was carried out using capacitors based on one-sided step junctions. For the case where the doping in the sandwiched N-region is much less than the P-layer dopings (i.e., $N_A >> N_D$), Equation (2.1) simplifies to:

$$Q = 2qN_D A(W - W_0) \qquad \text{for } N_A >> N_D \qquad (2.4)$$

and (2.2) reduces to:

$$W = \sqrt{\frac{2\varepsilon_S(V_{bi} + V_R)}{qN_D}} \qquad \text{for } N_A >> N_D \qquad (2.5)$$

As discussed in the introduction to this chapter, it is critical that the amount of charge a capacitor can store per unit area be maximized, as charge storage density greatly affects the size and performance of the complete DRAM chip. The combination of (2.4) and (2.5) immediately shows that:

$$Q \alpha (N_D)^{1/2} \qquad \text{for } N_A >> N_D \qquad (2.6)$$

Given a fixed N-layer voltage V_R, the charge density increases as the square root of the doping, so the charge density is optimized by maximizing the capacitor doping. Figure 2.4 shows the calculated dependence of P^+NP^+ capacitor charge density on N_D when the N-region is at +1 V. Equations 2.4 and 2.5 also imply that charge densities go up with N-layer bias, and this effect is documented in Figure 2.5.

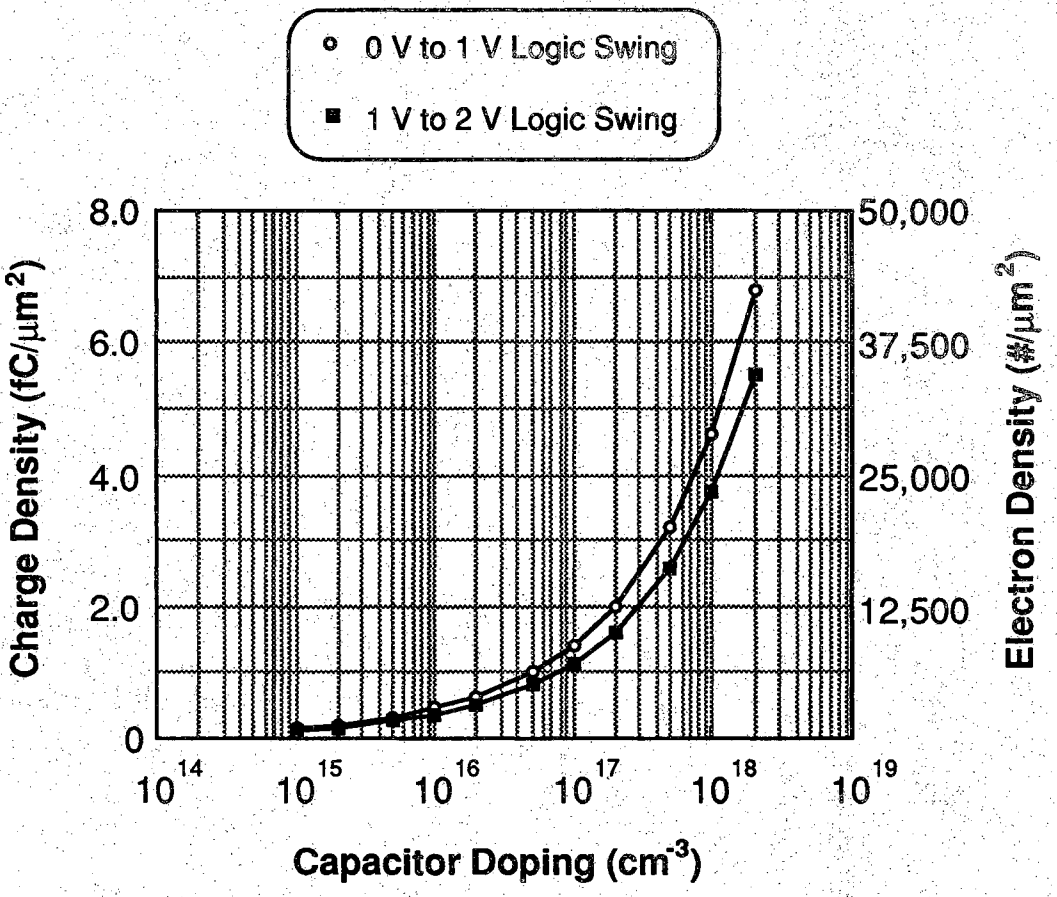


Figure 2.4 PNP capacitor charge density as a function of lighter-side doping. A P-layer doping of $N_A = 10^{19}$ cm^{-3}. Note that a 1 V to 2 V logic swing has a slightly lower charge density than a 0 V to 1 V logic swing.

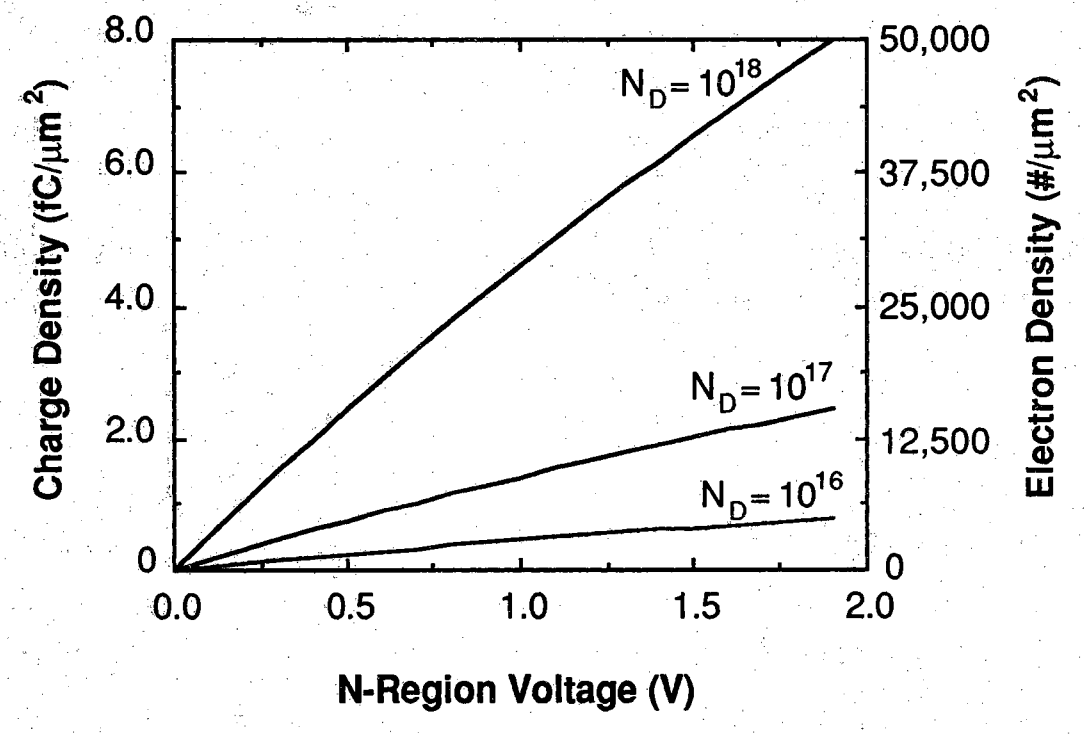


Figure 2.5 PNP capacitor charge density as a function of voltage. A P-layer doping of $N_A = 10^{19}$ cm^{-3} is assumed in the calculation.

2.1.3 PNP Capacitor Charge Measurement

The charge state of the PNP structure is monitored experimentally by measuring the device capacitance (Figure 2.6). For $t < -t_{PW}$ in Figure 2.6, the equilibrium capacitance is merely the zero-bias depletion capacitance of two PN junctions in series as depicted in Figure 2.3a. Following the application of the positive bias pulse ($t > 0$), both PN junctions are in reverse bias nonequilibrium as depicted in Figure 2.3c. The resulting increase in junction depletion width is witnessed by the measured capacitance at $t > 0$.

Under reverse bias, the measured AC small signal capacitance of a PN junction (C_J) will primarily be depletion capacitance [52,56]:

$$C_J = \frac{\varepsilon_S A}{W} \tag{2.7}$$

where ε_S is the semiconductor dielectric constant, A is the device area, and W is the depletion width. Recalling the assumption that the top and bottom P-layers were doped alike, the measured capacitance of the PNP structure C_{PNP} is the capacitance of the two identical junctions in series:

$$C_{PNP} = \frac{C_J}{2} = \frac{\varepsilon_S A}{2W} \tag{2.8}$$

The charge Q on the capacitor can be calculated using (2.8) to replace W and W_0 in (2.4):

$$Q = q\varepsilon_S A^2 N_D \left(\frac{1}{C_{PNP}} - \frac{1}{C_{PNP0}} \right) \tag{2.9}$$

where C_{PNP0} is the zero-charge equilibrium capacitance of the PNP structure.

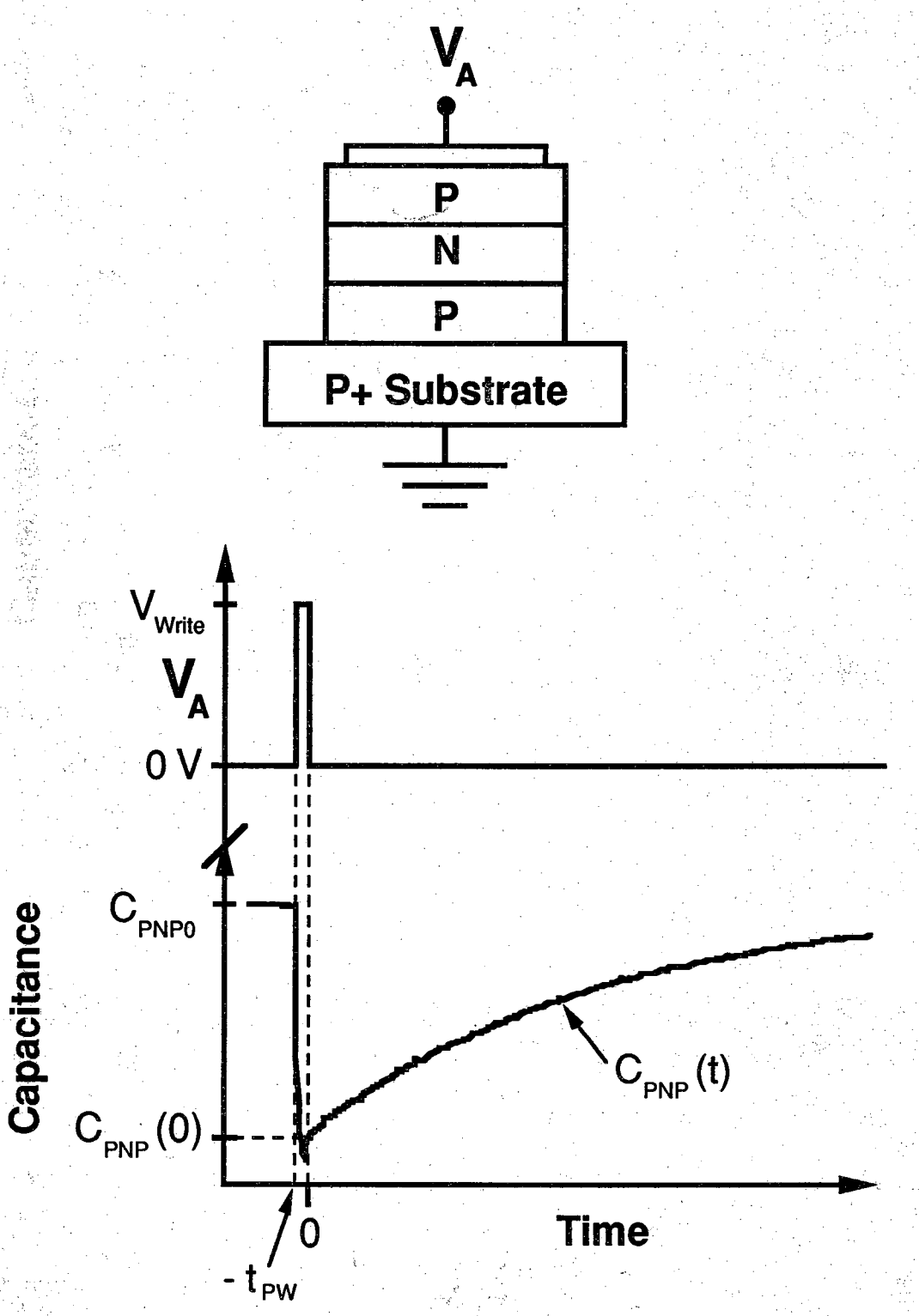


Figure 2.6 PNP capacitor storage time transient.

2.2 PNP Capacitor Charge Leakage Mechanisms

Ideally there would be no leakage currents in the PNP capacitor and it would retain the stored charge forever. However, actual devices eventually return to zero-bias equilibrium due to the leakage of charge through the reverse-biased PN junctions. For the device of Figure 2.6 this is witnessed by the eventual return of the capacitance to its initial value C_{PNP0} a while after bias pulse application. The reverse leakage current I_R will govern the charge decay of the device as:

$$\frac{dQ}{dt} = -I_R \tag{2.10}$$

For the voltages used in GaAs JFET and MESFET digital IC's ($|V| < 2$ V), this leakage is primarily due to thermal generation in the depletion regions. There is both a surface generation leakage current I_{PG} that scales with the perimeter of the device and a bulk generation leakage current I_{BG} that scales with the area of the device [1,2]:

$$I_R = I_{BG} + I_{PG} \tag{2.11}$$

Provided the junction has been properly fabricated, other sources of leakage current appear to be negligible at any appreciable reverse bias (Section 2.2.3) [1]. By minimizing these reverse bias leakage currents, the time that the capacitor retains stored charge is maximized.

2.2.1 Leakage Due to Bulk Generation

One of the primary sources of leakage current in a reverse-biased PN junction is thermal generation of electron-hole pairs at bulk defect centers in the depletion region. For the PN junction pictured in Figure 2.7 under reverse bias V_R the bulk generation leakage current is given by [52,56]:

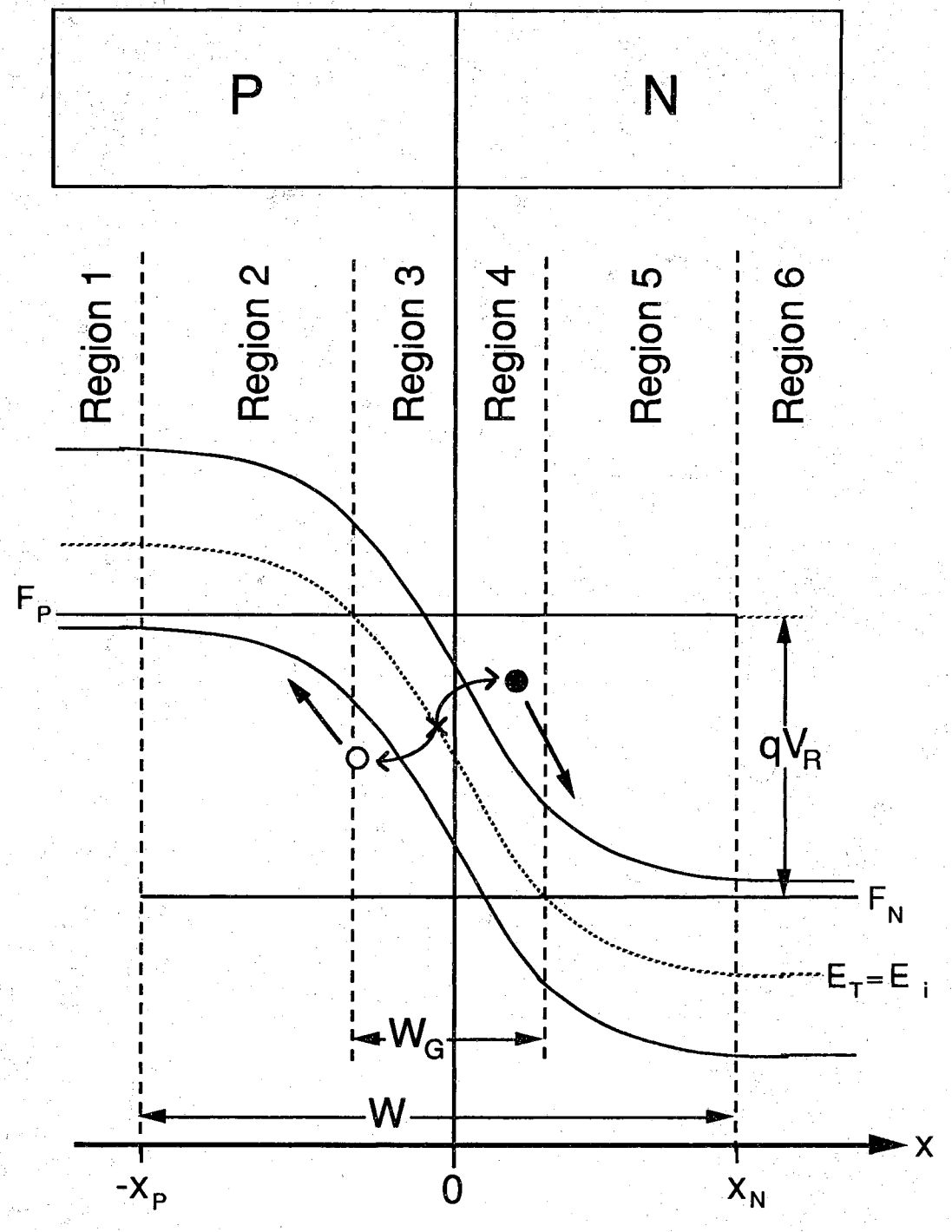


Figure 2.7 Reverse-biased PN junction band diagram.

$$I_{BG} = qA\int_{-x_N}^{x_P} G_B(x)\,dx \qquad (2.12)$$

where A is the area of the junction. The generation rate $G_B(x)$ describes the number of electron-hole pairs (ehp) per cm^3-sec produced by thermal generation at point x in the bulk depletion region. The bulk thermal generation rate due to centers at a single energy level E_T is given by [54]:

$$G_B(x) = \frac{n_i^2 - n(x)p(x)}{\tau_{pB}\left(n(x) + n_i e^{(E_T' - E_i)/kT}\right) + \tau_{nB}\left(p(x) + n_i e^{(E_i - E_T')/kT}\right)} \qquad (2.13)$$

where τ_{nB} and τ_{pB} are the hole and electron bulk generation lifetimes (sec), E_T' is the energy level of the centers adjusted for degeneracy, E_i is the intrinsic Fermi level, and n_i is the intrinsic carrier concentration. The carrier concentrations n(x) and p(x) are specified by:

$$n(x) = n_i e^{(F_N(x) - E_i(x))/kT} \qquad (2.14)$$

$$p(x) = n_i e^{(E_i(x) - F_P(x))/kT} \qquad (2.15)$$

where F_N and F_P are the electron and hole quasi-Fermi levels.

An analysis of (2.13) as a function of position in a reverse biased PN junction reveals that the vast majority of carriers will be generated in the region where $F_P > E_T' > F_N$ (Regions 3 & 4 of Figure 2.7). This can be seen through careful evaluation of (2.13) for each of the 6 regions of Figure 2.7. Under reverse bias the numerator of (2.13) is always less than n_i^2. The quasi-Fermi levels are constant across the depletion region, and reverse bias implies that $F_N - F_P$ is negative so that:

$$n(x)p(x) = n_i^2 e^{(F_N - F_P)/kT} = n_i^2 e^{-qV_R/kT} \qquad (2.16)$$

is negligible in the numerator of (2.13) for any appreciable reverse bias V_R. Thus the generation rate for regions 2-5 simplifies to:

$$G_B(x) = \frac{n_i}{\tau_{pB}\left(e^{(F_N - E_i(x))/kT} + e^{(E_T' - E_i)/kT}\right) + \tau_{nB}\left(e^{(E_i(x) - F_P)/kT} + e^{(E_i - E_T')/kT}\right)} \tag{2.17}$$

In region 5, $F_N > E_T'$ forces the electron exponential term of the denominator of (2.17) to grow large, so the generation rate becomes small. Similarly, the generation rate will be small for region 2 where $F_P < E_T'$. It is in regions 3 and 4 where $F_P > E_T' > F_N$ that the generation rate $G_B(x)$ takes on a significant value.

Since the vast majority of electron-hole pair generation takes place in Regions 3 and 4, it is naturally referred to as the generation width W_G. The generation rate within W_G is essentially independent of position:

$$G_B = \frac{n_i}{\tau_{pB}e^{(E_T' - E_i)/kT} + \tau_{nB}e^{(E_i - E_T')/kT}} \tag{2.18}$$

When τ_{nB} and τ_{pB} are within about two orders of magnitude of each other, the exponentials in the denominator of (2.18) strongly favor R-G centers that are near E_i in energy. If the majority of bulk generation takes place through near-midgap R-G centers, the bulk generation rate becomes:

$$G_B = \frac{n_i}{\tau_{pB} + \tau_{nB}} \tag{2.19}$$

Since most electron-hole pairs are being generated in W_G, and the generation rate is independent of position within W_G, (2.12) can be simplified to:

$$I_{BG} = qAG_BW_G \tag{2.20}$$

The validity of this expression for a symmetrically doped ($N_A = N_D$) junction is demonstrated by Figure 2.8, which compares J(x) calculated directly from full evaluation of (2.12) and (2.13) based on midgap generation with J(x) calculated from (2.19) and (2.20) [1].

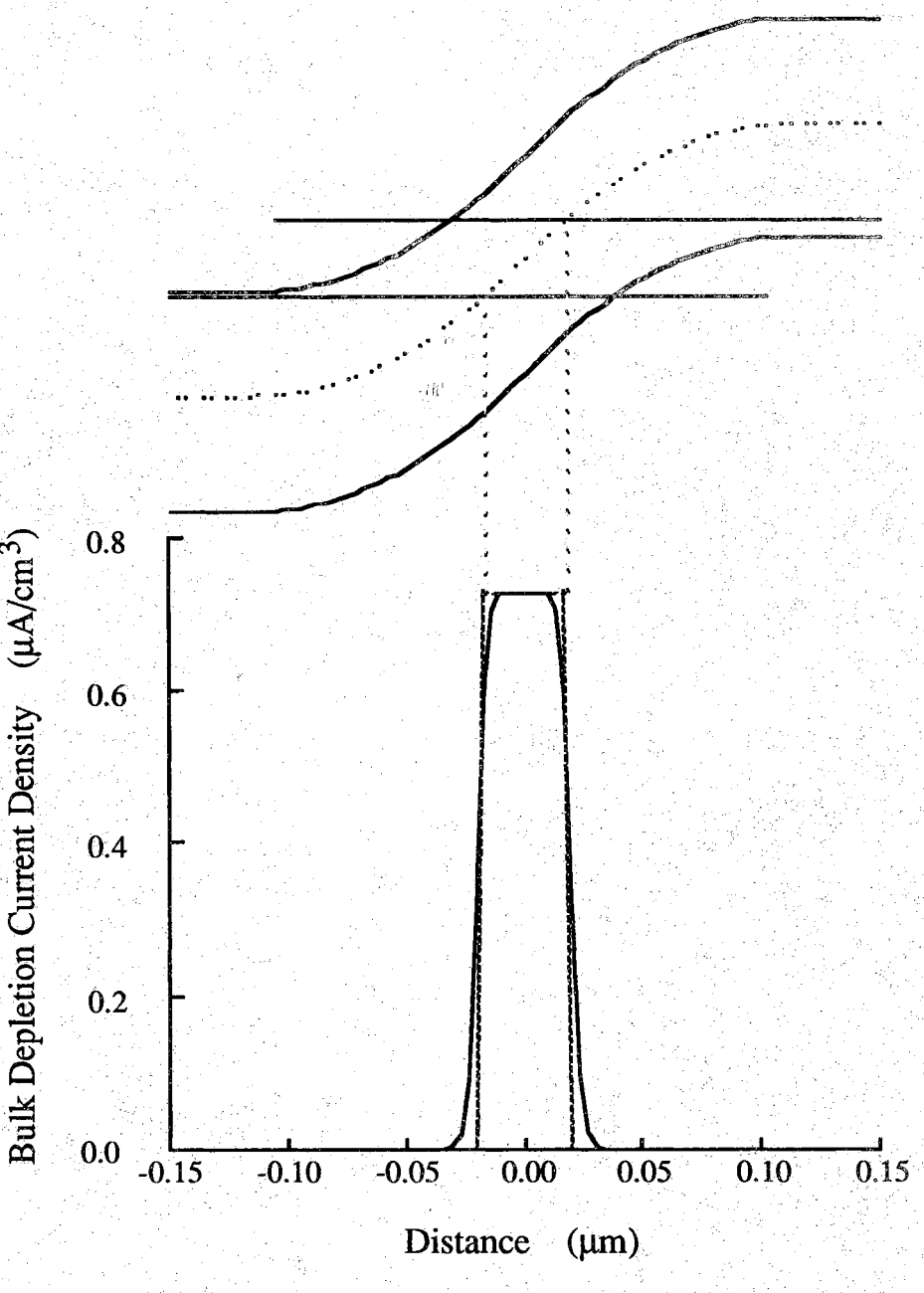


Figure 2.8 Simulated bulk generation current in a PN junction. The solid curve represents a full evaluation of (2.13), while the dashed rectangle represents the leakage current approximation of (2.20). The calculation parameters are $N_A = N_D = 10^{17}$ cm^{-3}, $V_R = 0.5$ V, and $\tau_{nB} = \tau_{pB} = 10^{-7}$ sec. After Reference [1].

At zero bias the depletion region is at its equilibrium width W_0 and there is no net generation-recombination current. When a reverse bias is applied, the depletion width widens and generation current is produced. It therefore follows that the generation width W_G can be approximated to first order by [1]:

$$W_G \cong W - W_O = \left[\frac{2\varepsilon_S}{q}\frac{(N_A + N_D)}{N_A N_D}\right]^{1/2}\left[(V_{bi} + V_R)^{1/2} - (V_{bi})^{1/2}\right] \quad (2.21)$$

Since W_G is function of both doping and applied reverse bias voltage V_R, the bulk reverse bias leakage I_{BG} is also a function of doping and voltage.

It should be noted that (2.21) is only a first-order approximation for the effective generation width. In one-sided junctions ($N_A >> N_D$ or $N_D >> N_A$), the effective generation width (i.e., the region where $F_P > E_T' > F_N$) is larger than what is predicted by the $W - W_0$ approximation in (2.21) [1]. A detailed discussion of this phenomenon is left to Reference 3, but its net effect is always less than a factor of two so it is considered only as a second-order effect.

2.2.2 Leakage Due to Surface Generation

The second major source of reverse bias generation current occurs at the surface of the PN junction along the perimeter of the device. This generation is governed by surface states according to [15,54]:

$$G_P = \left[\int_{Ev}^{Ec} \frac{c_{ns}c_{ps}D_{IT}(E)dE}{c_{ns}e^{(E - E_i)/kT} + c_{ps}e^{(E_i - E)/kT}}\right] n_i \quad (2.22)$$

where c_{ns} and c_{ps} are the surface hole and electron capture coefficients ($cm^3\ sec^{-1}$), and $D_{IT}(E)$ is the surface state density ($cm^{-2}\text{-}eV^{-1}$). The assumption is often made that midgap surface states are dominant, in which case the perimeter generation rate simplifies to [15,54,115]:

$$G_P = s_o n_i \qquad (2.23)$$

where s_o is the surface generation velocity (cm/sec).

Exact calculation of surface generation current is excruciatingly difficult due to trap-induced Fermi level pinning at the GaAs surface. Despite these complications, there are parallels to the bulk generation arguments presented in the previous section. A detailed discussion and calculation of the surface generation current is given in Reference 1. The resulting first-order approximation for surface generation current in a reverse biased GaAs PN junction is [1]:

$$I_{PG} \cong qG_P W_G P \qquad (2.24)$$

where G_P is the perimeter generation rate (ehp/cm^2-sec) and P is the length of the etched capacitor perimeter. As one might intuitively expect from parallel bulk generation arguments, the surface generation current is proportional to the generation width. A full calculation of (2.22) done in Reference 1 reveals that (2.24) is not as accurate as the bulk depletion current approximation (Figure 2.9).

2.2.3 Other Leakage Mechanisms

The leakage of charge due to other leakage mechanisms is insignificant compared to generation current for the reverse biases of interest. In GaAs the extremely low equilibrium minority carrier concentrations result in a vanishingly small concentration gradient in the neutral regions under reverse bias, and this in turn makes the bulk diffusion current negligibly small [1]. Surface diffusion current is enhanced somewhat by the fact that Fermi-level pinning causes increased minority carrier concentrations at the surface. However, using reasonable assumptions for GaAs surface-state parameters, the surface diffusion current was calculated to be insignificant compared to generation for biases greater than 0.1 V [1,116].

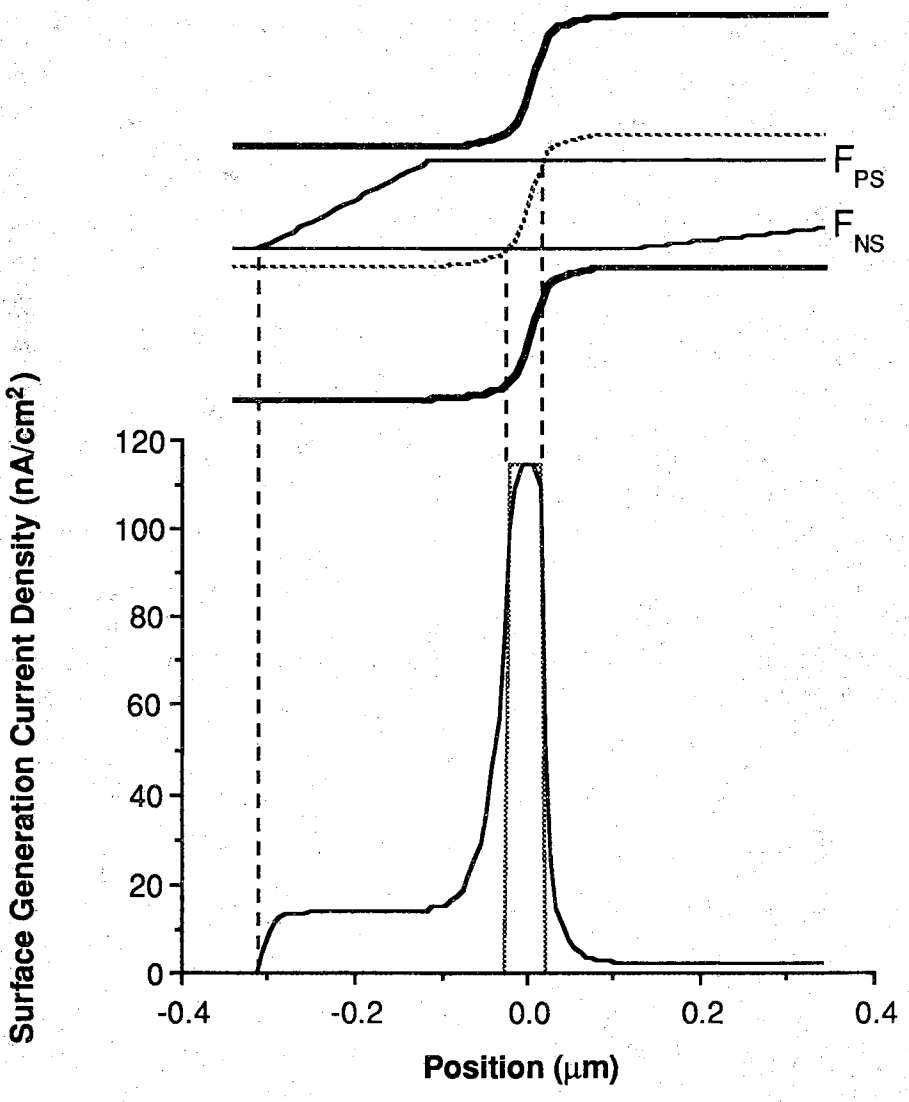


Figure 2.9 Simulated perimeter generation current in a PN junction. The solid curve represents a full calculation of (2.22), while the dashed rectangle represents the leakage current approximation of (2.24). The calculation parameters are $N_A = N_D = 10^{17}$ cm^{-3}, $V_R = 0.5$ V, and $s_o = 4 \times 10^5$ cm/sec. After Ref. [1].

Electrically active point defects, such as oval growth defects or spiking of metal contacts through the junction, will naturally damage the diode. Most diodes found to contain such defects were rectifying, but the reverse leakage current was typically larger by a few orders of magnitude. These kinds of defects are considered to be a process yield problem, which is not part of this work. PNP capacitors that were recognized as having such faults were discarded and no data from them is presented or discussed further.

2.3 PNP Capacitor Storage Time Theory

Now that the PNP capacitor has been introduced and the physical mechanisms which will govern its storage time have been discussed, a proper investigation into its dynamic behavior is in order. Section 2.3.1 presents the theoretical basis for charge loss in a PNP capacitor using the generation current mechanisms described previously in Section 2.2. Section 2.3.2 discusses the scaling of storage times with device geometry that arises from bulk and perimeter generation mechanisms. Sections 2.3.3 and 2.3.4 draw simple connections between the I-V characteristics of a PN junction and corresponding PNP capacitors storage times. Section 2.3.5 discusses the dependence of storage time on device doping profile.

2.3.1 Storage Time Transient Theory

Consider a PNP storage capacitor that has already had a positive charge written to it by a bias pulse (Figure 2.3c). The charge Q on a PNP capacitor with $N_A >> N_D$ given in (2.4) can be expressed in terms of the (2.21) approximation for W_G:

$$Q = 2qAN_DW_G \tag{2.25}$$

The rate at which charge leaks out of the PNP capacitor is given by the total reverse-bias generation current. The total generation current from one junction is given by the combination of (2.11), (2.20), and (2.24):

$$I_R = I_{BG} + I_{PG} = qAG_BW_G + qG_PW_GP \tag{2.26}$$

Since we have two PN junctions in the PNP capacitor structure:

$$\frac{dQ}{dt} = -2I_R = -2I_{BG} - 2I_{PG} = -2qAW_GG_B - 2qPW_GG_P \tag{2.27}$$

The voltage dependent W_G can be expressed in terms of the charge by rearranging (2.25):

$$W_G = \frac{Q}{2qAN_D} \tag{2.28}$$

Using (2.28) to substitute for W_G in (2.27) a first-order linear differential equation can be obtained:

$$\frac{dQ}{dt} = -\frac{Q}{N_D}\left(G_B + \frac{P}{A}G_P\right) \tag{2.29}$$

The time solution of (2.29):

$$Q(t) = Q(0)e^{\frac{-(G_B + (P/A)G_P)}{N_D}t} = Q(0)e^{-t/\tau_S} \tag{2.30}$$

is a decaying exponential function with a time constant of τ_S, where:

$$\tau_S = \frac{N_D}{G_B + \frac{P}{A}G_P} \tag{2.31}$$

The above result is the first-order theoretical storage time of a PNP capacitor with $N_A >> N_D$.

It should be noted that the above derivation is a first-order result based on a number of first-order approximations. There are numerous second-order effects, some of which are outlined in this chapter and in Reference 1. Among these are non-exponential charge recovery transients and dependence of τ_S on bias pulse magnitude. Nevertheless the experimental results of Section 2.7.1 demonstrate that this first-order derivation is an acceptable representation of what is physically occurring in most of the PNP capacitors examined in this work.

2.3.2 Dependence of Storage Time on Device Lateral Geometry

The above results have some important implications. The most obvious is that the capacitor storage time can be dominated either by bulk generation or surface generation, or there can be significant contributions from both. If the capacitors on a given wafer are all bulk dominated (i.e., $G_B >> (P/A)G_P$ for all devices), the storage times will be constant and not change with capacitor size:

$$\tau_S = \frac{N_D}{G_B} \tag{2.32}$$

If on the other hand the capacitors are all perimeter dominated (i.e., $G_B << (P/A)G_P$ for all devices), the storage times will vary with planar geometry as the inverse of perimeter-to-area ratio:

$$\tau_S = \frac{N_D}{G_P}\left(\frac{A}{P}\right) \tag{2.33}$$

The storage times of perimeter-dominated devices will decrease as device sizes shrink due to the increase in perimeter-to-area ratio. Say for example the length of the sides of a given square capacitor are cut in half. The new area will be 1/4 of the previous area while the perimeter is reduced to 1/2

its previous value. The new P/A is twice the original value, so one should expect a smaller perimteter-dominated capacitor to have half the storage time of the large capacitor.

The relative importance of bulk and perimeter generation can be ascertained by plotting $1/\tau_S$ as a function of device perimeter-to-area ratio:

$$\frac{1}{\tau_S} = \frac{G_P}{N_D}\frac{P}{A} + \frac{G_B}{N_D} \qquad (2.34)$$

The above relation is nothing more than (2.31) re-written in the familiar y = mx + b linear form. By plotting the inverse storage times of various sized capacitors from the same wafer and fitting it to a line, G_P can be extracted from the slope while G_B can be calculated from the y-intercept. In addition to providing valuable insight into the relative importance of bulk and surface leakage mechanisms, this data can be used to predict the storage time of any sized device on the wafer.

The scaling phenomena outlined above dictates that direct comparison of measured storage times between two separate wafers is consistent only when devices with like P/A are considered. Capacitors with unlike doping profiles will have different generation widths, so storage times will differ even if both wafers have the same generation rates. In light of this fact, the generation rates themselves are the fairest basis of comparison when analyzing wafer material quality.

2.3.3 The Capacitor Storage Time to Diode Current Relation

Because the storage time of a PNP capacitor is determined by the reverse leakage of the PN junctions, a direct relationship between reverse-biased diode current density J_R and capacitor storage time τ_S can be easily derived. An approximation for the reverse biased current density of a PN junction is obtained by dividing (2.26) by the junction area:

$$J_R = J_{BG} + J_{PG} = qW_G\left(G_B + \frac{P}{A}G_P\right) \qquad (2.35)$$

The combination of (2.31) and (2.35) yields an approximate relation for the leakage current density of the junctions of the PNP capacitor in terms of the capacitor's storage time:

$$J_R = \frac{qW_G N_D}{\tau_S} \tag{2.36}$$

Equation (2.36) allows one to predict the storage time of a symmetric PNP storage capacitor from the measured reverse leakage of a PN junction diode with identical junctions and planar layout geometry. Conversely, knowing the storage time of a symmetric PNP capacitor, one can estimate the reverse-bias leakage of an analogous diode.

This concept was verified experimentally by the data presented in Section 2.7.3 [4]. Due to second-order effects (bias pulse variation of τ_S [1]), this approximation has the limitation that the bias pulse applied to measure the storage time be in the neighborhood of the voltage used to measure the reverse current density, and of course it only applies between devices with like P/A ratios.

2.3.4 Worst-Case Storage Time Approximation

A worst-case linear storage time approximation can quickly be obtained by measuring the leakage current of a capacitor diode at the voltage applied during a write pulse ($I_R(V_{Write})$). By assuming the leakage out of the capacitor is constant and not a function of voltage:

$$\frac{dQ}{dt} = -2I_R(V_{Write}) = \text{Constant} \tag{2.37}$$

The factor of two accounts for top and bottom junctions leakage. Relation (2.37) represents a conservative leakage estimate because the voltage on the storage node at $t = 0^+$ will actually be less than V_{Write}. One can easily obtain an expression for the charge remaining in the capacitor as a function of time:

$$Q(t) = Q(0) - 2I_R t \tag{2.38}$$

Since τ_S is defined as the time after which 1/e of the original charge is left, the worst case approximation for the storage time becomes:

$$\tau_S \cong \frac{Q(0)\left(1 - \frac{1}{e}\right)}{2I_R} \tag{2.39}$$

The actual storage time is guaranteed to be longer than the linear approximation because the actual leakage current decreases with voltage, and the storage node voltage is less than V_{Write}.

2.3.5 Numerical Simulation of Storage Time Transients

The storage time transient theory of Section 2.3.1 is based on several approximations that are accurate to first order. However, if one chooses to build capacitors out of diode structures that seriously compromise the validity of these approximations, the charge decay may become highly non-exponential. In these cases capacitor charge decay can be computed directly based on theoretical or measured diode I-V characteristics using a simple timestep computational simulation technique.

The charge Q on the capacitor at any time t can be used to calculate the voltage V_R across the capacitor diode junctions (via (2.1) and (2.2) for the PNP capacitor). Using either theoretical or measured diode I-V characteristics, a leakage current I_R can be obtained from the voltage, and this leakage current in turn is used to calculate the amount of charge that leaves the capacitor over timestep Δt:

$$\frac{dQ}{dt} = I_R(V_R) \tag{2.40}$$

Thus a simple computational loop based on:

$$Q(t + \Delta t) = Q(t) - I_R(V_R(Q(t)))\,\Delta t \qquad (2.41)$$

can be set up to calculate the charge decay transient. This numerical technique can be applied to any diode junction capacitor structure, regardless of the physical mechanisms dominating charge leakage.

2.4 Theoretical Effect of Doping Profile

It has already been shown that charge density increases with capacitor doping (Section 2.1.2). Capacitor storage times are also directly affected by the junction doping profile. Equation (2.31) suggests that capacitor storage times will increase directly with lighter-side doping. This effect arises from the combination of decreased generation width W_G in (2.21) and the increased charge storage density of (2.25).

There are limits however to the storage time advantage gained by increased doping. As the lighter side doping is increased to degenerate levels, the depletion width shrinks (Figure 2.10) and built-in electric fields swell (Figure 2.11) to the point where other physical leakage mechanisms, such as tunneling, avalanching, and field-enhanced generation, could increase junction leakage [1,2,52,56].

2.4.1 Field-Enhanced Generation

It turns out that the primary parasitic leakage mechanism in highly doped PN junctions at the reverse biases of interest ($|V_R| < 2$ V) is field-enhanced thermal generation occurring in the bulk material [1,2]. As depicted by Figure 2.12, the field enhanced generation phenomenon is nothing more than thermal generation that has been enhanced by the presence of a large electric field [99,100]. Carriers at a generation site must escape the Coulombic spatial potential of the center to carry leakage current. The presence of a strong electric field alters the shape of the potential, effectively lowering the barrier carriers must surmount to

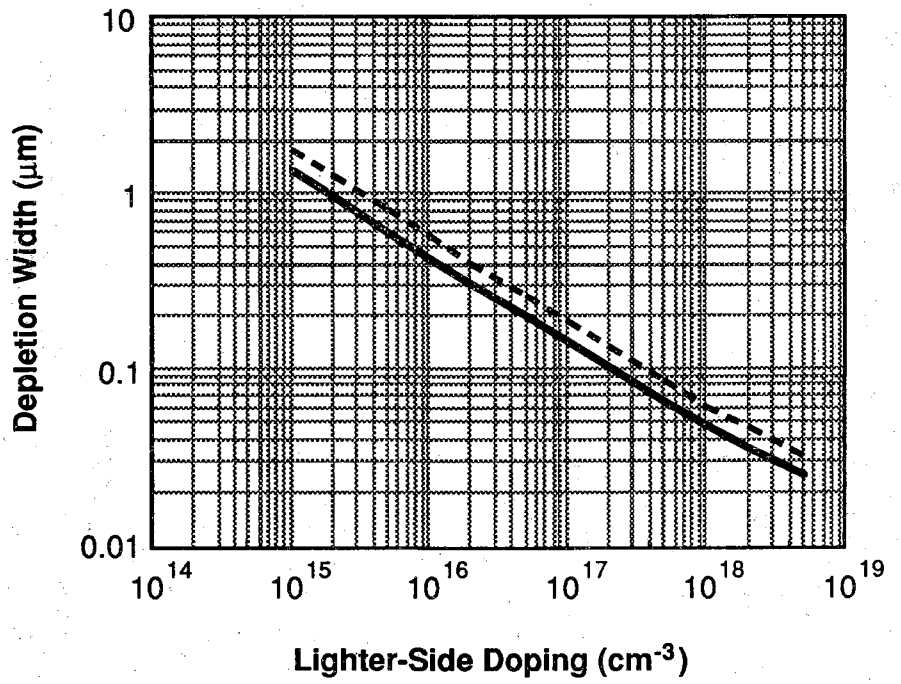


Figure 2.10 PN junction depletion width as a function of lighter-side doping. The solid line represents the equilibrium depletion width, while the dotted line is the depletion at 1V reverse bias. The calculation was carried out assuming a step junction with $N_A = 10^{19}$ cm^{-3}.

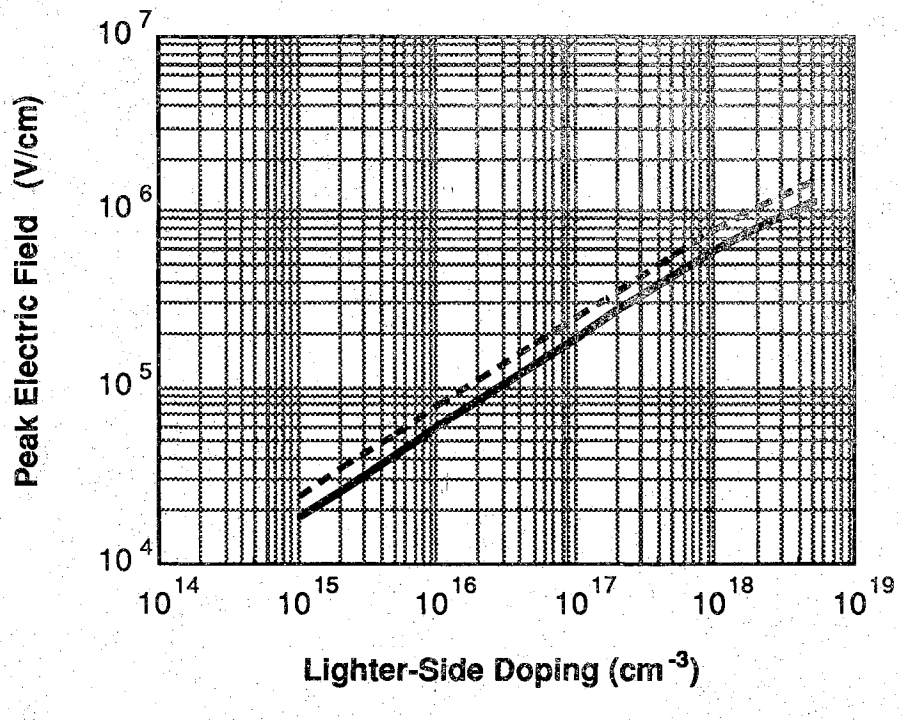


Figure 2.11 PN junction peak electric field as a function of lighter-side doping. The solid line represents the equilibrium peak field, while the dotted line is ε_{Peak} at 1V reverse bias. The calculation was carried out assuming a step junction with $N_A = 10^{19}$ cm^{-3}.

become mobile. This phenomena, also referred to as the Frenkel-Poole effect [99,100], causes the bulk generation carrier lifetimes τ_{nB} and τ_{pB} to be a function of electric field. For reasons given in Reference 1, field-enhancement does not significantly affect surface generation.

A simple one-dimensional approximate model for barrier lowering was derived by Frenkel [99]:

$$\Delta E = 2\sqrt{\frac{q\varepsilon}{\pi\varepsilon_S}} \tag{2.42}$$

where ΔE is the barrier lowering in eV, ε_S is the high-frequency semiconductor dielectric constant in F/cm, and ε is the electric field in V/cm. Figure 2.13 plots the barrier reduction ΔE in GaAs as a function of the electric field calculated from (2.42). Following model for thermionic emission of carriers over a potential barrier, the dependence of τ_{nB} and τ_{pB} on electric field ε could be modelled by [100]:

$$\tau = \tau(\varepsilon = 0)\, e^{-\Delta E/kT} = \tau(\varepsilon = 0) \exp\left(\frac{-2}{kT}\sqrt{\frac{q\varepsilon}{\pi\varepsilon_S}}\right) \tag{2.43}$$

The carrier lifetimes that affect bulk generation are exponentially dependent on the square root of the electric field. Since the electric field within a PN junction is a function of position, complete modelling of $G_B(x)$ within the framework of (2.13) would have to include position-dependent carrier lifetimes $\tau_{nB}(x)$ and $\tau_{pB}(x)$.

In silicon the field-enhanced theory given above has been found to greatly overestimate the experimentally observed effect [100,117,118]. Nevertheless, equations (2.42) and (2.43) qualitatively represent the physics of field-enhanced generation that is observed in heavily doped PN junction storage capacitors. The exponential dependence of τ_{nB} and τ_{pB} on electric field via (2.43) implies that undesired field-enhanced generation is its greatest where $|\varepsilon(x)|$ is a maximum. As capacitor junction doping increases towards degenerate levels, the storage time advantage suggested by (2.31) will at some point be negated by field-enhance generation from increased

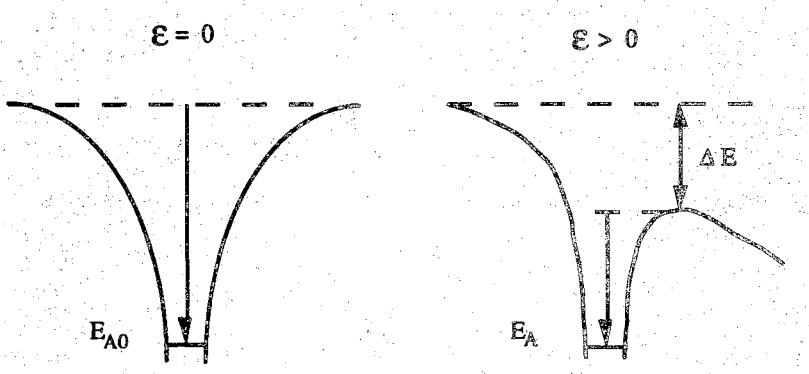


Figure 2.12 1-D pictorial representation of field-enhanced barrier lowering. The Coulombic potential of a generation site is altered by the electric field causing a reduction in the effective barrier height. After Refs. [1,100].

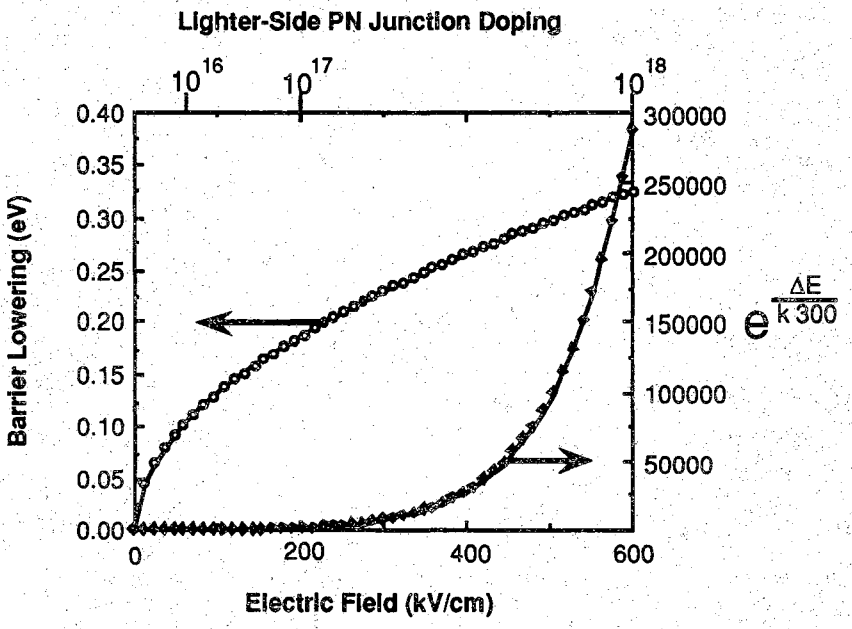


Figure 2.13 Barrier lowering as a function of electric field. The left axis shows the theoretical barrier lowering from (2.42), while the right axis shows the corresponding thermionic emission factor from (2.43). The top axis is a reference to the peak PN junction built-in fields for the lighter-side dopings shown.

built-in junction fields (Figure 2.11). Experimental documentation of this effect for GaAs PNP capacitors is presented in Section 2.7.

2.5 PiN Junction Capacitors

The detrimental leakage mechanisms associated with the high built-in field and narrow depletion width of a heavily-doped junction can be alleviated somewhat by the introduction of a thin undoped layer between the heavily doped P and N regions, or in other words switch from a pure PN junction to a PiN junction. The insertion of the i-layer widens the depletion region some, but it also reduces the magnitude of the electric field across the junction to cut down on field-enhanced generation leakage. Unfortunately it also results in a charge density penalty, as device capacitance is decreased by the widening of the depletion region.

A quantitative understanding of PiN junction physics is needed to properly evaluate the storage time versus charge density trade-off. This section presents a comprehensive discussion of relevant PiN junction theory as it applies to GaAs charge storage capacitors. Section 2.5.1 derives quantitative PiN junction electrostatics within the framework of the depletion approximation. Section 2.5.2 discusses the leakage characteristics of PiN junctions, and concludes that PiN junction leakage can be approximated to first order by the PN junction leakage physics of Section 2.2. Finally, theoretical PiN capacitor performance trade-offs are discussed in Section 2.5.3.

2.5.1 PiN Junction Electrostatics

The PiN junction is very similar in nature to a PN junction. Most of the physical differences between PN and PiN junctions can be understood through the graphical representations of junction electrostatics is given in Figure 2.14. The N and P dopings are taken to be the same for both structures, and the unintentional background i-layer doping is much less than N_A and N_D and taken to be zero. Because there is no difference

between the neutral region Fermi levels, the built-in junction voltage V_{bi} given by (2.3) is the same for both junctions. Under the same applied bias V_A, the integral of the electric field for both structures must therefore also be equal [52,56]:

$$(V_{bi} - V_A)_{PN} = (V_{bi} - V_A)_{PiN} = -\int_{-\infty}^{+\infty} \varepsilon(x)\, dx \qquad (2.44)$$

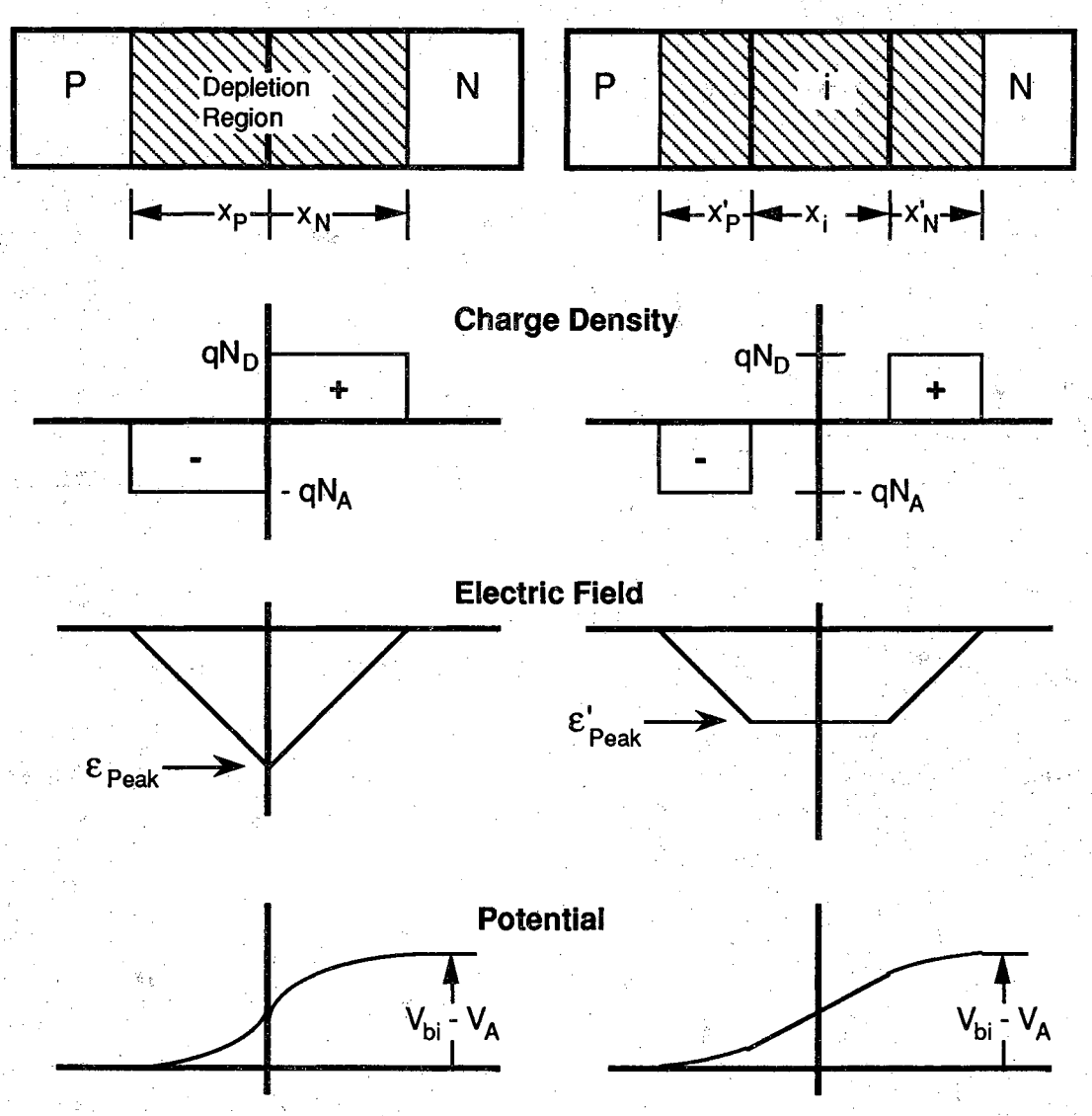
As can be seen in Figure 2.14, there are clear similarities between the electrostatics of the doped regions of both junctions. Aside from the i-region, the electric profiles of the PN junction and PiN junction are essentially the same. The only difference in $\varepsilon(x)$ for the PiN diode doped-regions and $\varepsilon(x)$ for the PN diode is the disparity in peak electric field. This disparity arises from the voltage drop across the i-layer V_i which is given by:

$$V_i = -\varepsilon'_{Peak}\, x_i \qquad (2.45)$$

Since ε_{Peak} in Figure 2.14 is a negative quantity, V_i defined in the above manner is positive. The electrostatics of biased PN junctions can be derived from zero-bias equations by simply replacing V_{bi} with $V_{bi} - V_A$ [52]. Similarly, one can calculate the PiN diode doped-region electric profiles from analogous PN junction equations shifted by $-V_i$. For example, the sum of x'_N and x'_P in the PiN diode (Figure 2.14b) under bias V_A is the depletion width of the analogous PN diode (Figure 2.14a) under applied bias $V_A - V_i$. The depletion width of a PN junction under applied bias V_A is [52]:

$$W = x_N + x_P = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} - V_A)} \qquad (2.46)$$

Using the above arguments one can write a doped-region depletion width W' for the PiN device using the PN junction equation shifted by V_i:



a) PN Junction b) PiN Junction

Figure 2.14 Comparison of PN and PiN junction electrostatics. Both structures are assumed to have the same N and P doping concentrations.

$$W' \equiv x'_N + x'_P = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} - V_A - V_i)} \qquad (2.47)$$

Note that W' is the depletion in the doped regions of the PiN device, and not the total depletion width of the PiN device. The total depletion width of the PiN junction is given by (Figure 2.14b):

$$W_{PiN} = W' + x_i = x'_N + x'_P + x_i \qquad (2.48)$$

The ratio of W to W' can be calculated from (2.46) and (2.47):

$$\frac{W}{W'} = \frac{\sqrt{V_{bi} - V_A}}{\sqrt{V_{bi} - V_A - V_i}} \qquad (2.49)$$

Application of similar arguments to x_N and x_P leads to:

$$\frac{x_N}{x'_N} = \frac{x_P}{x'_P} = \frac{\sqrt{V_{bi} - V_A}}{\sqrt{V_{bi} - V_A - V_i}} \qquad (2.50)$$

The peak electric field in the PN junction is given by [52]:

$$\varepsilon_{Peak} = \frac{qN_D x_N}{\varepsilon_S} = \frac{qN_A x_P}{\varepsilon_S} \qquad (2.51)$$

while the peak electric field in the PiN junction is:

$$\varepsilon'_{Peak} = \frac{qN_D x'_N}{\varepsilon_S} = \frac{qN_A x'_P}{\varepsilon_S} \qquad (2.52)$$

The ratio of ε_{Peak} to ε'_{Peak} from the previous three equations is:

$$\frac{\varepsilon_{Peak}}{\varepsilon'_{Peak}} = \frac{\sqrt{V_{bi} - V_A}}{\sqrt{V_{bi} - V_A - V_i}} \qquad (2.53)$$

Using the definitions of Figure 2.14, the voltage drop across the PN junction in terms of the peak PN electric field ε_{Peak} is [52]:

$$(V_{bi} - V_A)_{PN} = \frac{1}{2} x_P \varepsilon_{Peak} + \frac{1}{2} x_N \varepsilon_{Peak} \tag{2.54}$$

while the voltage drop across the PiN junction in terms of the peak PiN electric field ε'_{Peak} is:

$$(V_{bi} - V_A)_{PiN} = \frac{1}{2} x'_P \varepsilon'_{Peak} + \frac{1}{2} x'_N \varepsilon'_{Peak} + x_i \varepsilon'_{Peak} \tag{2.55}$$

Since (2.54) and (2.55) must be equal according to (2.44):

$$\frac{1}{2} x_P \varepsilon_{Peak} + \frac{1}{2} x_N \varepsilon_{Peak} = \frac{1}{2} x'_P \varepsilon'_{Peak} + \frac{1}{2} x'_N \varepsilon'_{Peak} + x_i \varepsilon'_{Peak} \tag{2.56}$$

The above equation can be re-written in terms of the depletion widths defined in (2.46) and (2.47):

$$\frac{1}{2} W \varepsilon_{Peak} = \left(\frac{1}{2} W' + x_i\right) \varepsilon'_{Peak} \tag{2.57}$$

Replacing W' and ε_{Peak} using relations (2.49) and (2.53):

$$\frac{1}{2} W \frac{\sqrt{V_{bi} - V_A}}{\sqrt{V_{bi} - V_A - V_i}} \varepsilon'_{Peak} = \frac{1}{2} W \frac{\sqrt{V_{bi} - V_A - V_i}}{\sqrt{V_{bi} - V_A}} \varepsilon'_{Peak} + x_i \varepsilon'_{Peak} \tag{2.58}$$

Substitution of (2.46) for W and (2.45) for V_i and algebraic simplification produces:

$$\frac{1}{2} \sqrt{\frac{2\varepsilon_S}{q} \left(\frac{N_A + N_D}{N_A N_D}\right)} x_i (\varepsilon'_{Peak})^2 + \sqrt{V_{bi} - V_A + \varepsilon'_{Peak} x_i}\, \varepsilon'_{Peak} x_i = 0 \tag{2.59}$$

The trivial $\varepsilon'_{Peak} = 0$ solution to (2.59) can be discarded yielding:

$$\frac{1}{2}\sqrt{\frac{2\varepsilon_S}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)}\,\varepsilon'_{Peak} + \sqrt{V_{bi} - V_A + \varepsilon'_{Peak} x_i} = 0 \qquad (2.60)$$

Given layer dopings, i-region thickness, and applied junction voltage, (2.60) can be quadratically solved for $\varepsilon'_{Peak} < 0$. Once the peak PiN electric field ε'_{Peak} is known, the junction distributions $\rho(x)$, $\varepsilon(x)$, and $V(x)$ in Figure 2.14b can be calculated in a straightforward manner.

Figures 2.15 and 2.16 show PiN junction design curves calculated from the above relations. For heavily doped junctions an i-layer thickness of several 100 Å more than halves the peak built-in electric field (Figure 2.16), but it also causes an increase in overall depletion width (Figure 2.15). Figure 2.17 shows that the ε'_{Peak} increases somewhat upon the application of reverse bias, but at the small biases ($V_R < 2V$) proposed for GaAs DRAM applications the majority of the field is built-in in nature.

2.5.2 PiN Junction Leakage

This section discusses the leakage physics of the PiN junction, which turns out to be nearly identical to PN junction. As with the PN junction, the primary source of leakage is thermal generation of electron-hole pairs in the depletion region. Excluding field-enhanced generation effects, arguments analogous to those in Section 2.2 can be presented that lead to a nearly constant generation rate over a given generation width. This is demonstrated by the calculation of Figure 2.18, which uses (2.13) with a full band structure obtained from the PiN junction electrostatics outlined in the previous section. Because generation in the PiN junction is essentially constant across a generation width W_G, the bulk leakage current is adequately approximated by the bulk PN junction leakage expression given in (2.20).

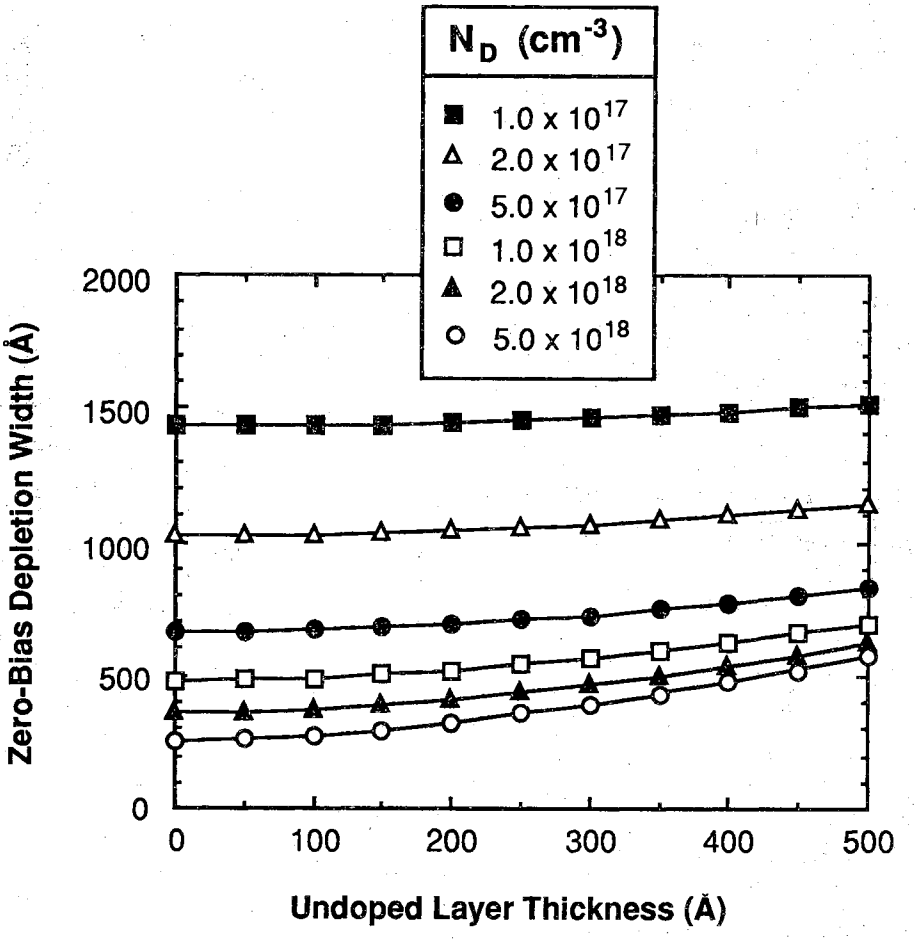


Figure 2.15 PiN junction depletion width as a function of i-layer thickness. A P^+iN junction with $N_A = 2.0 \times 10^{19}$ cm^{-3} was assumed for the calculation.

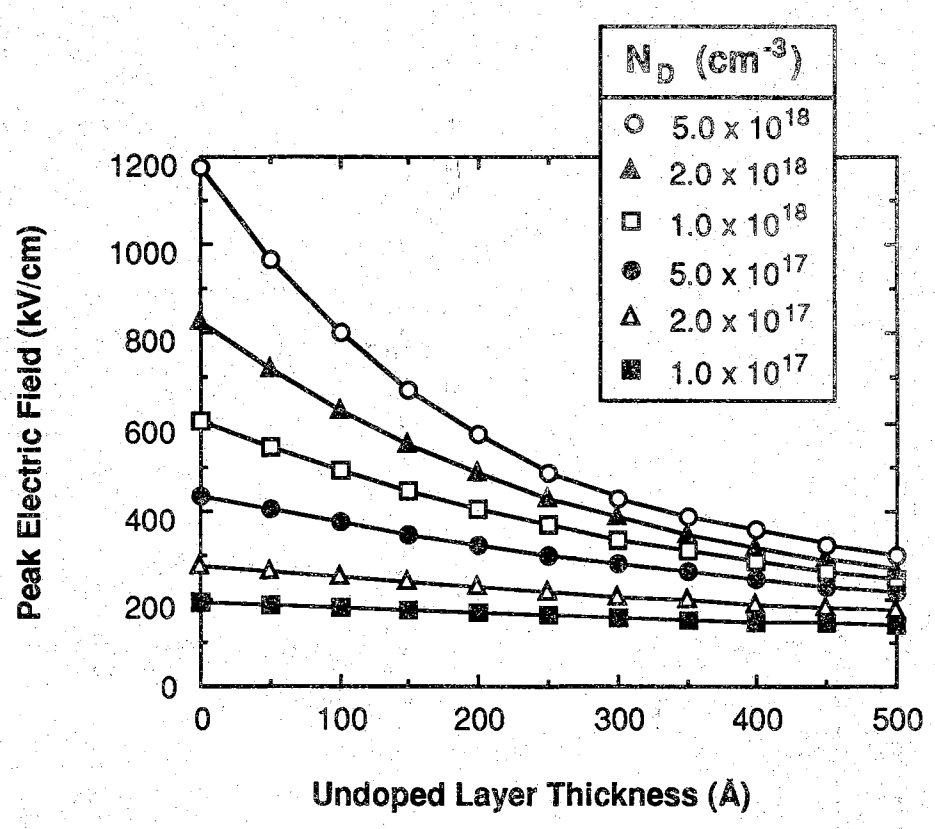


Figure 2.16 PiN junction peak electric field as a function of i-layer thickness. A P^+iN junction with $N_A = 2.0 \times 10^{19}$ cm^{-3} was assumed for the calculation.

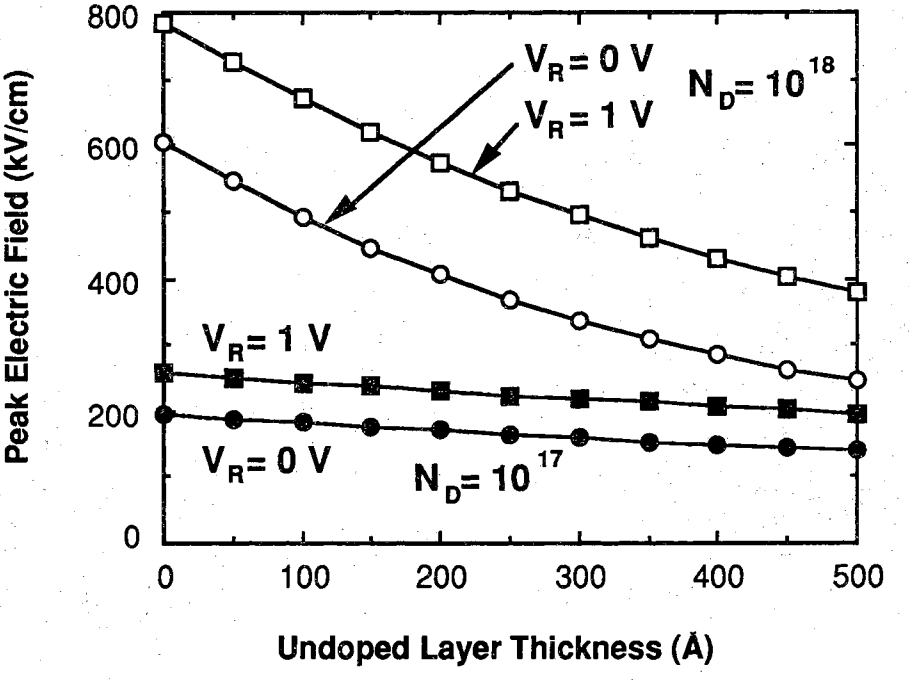


Figure 2.17 Comparison of PiN junction peak electric field between V_R = 0 and 1V. Under the reverse biases of interest, the majority of the electric field is built-in in nature. A P^+iN junction with $N_A = 2.0 \times 10^{19}$ cm^{-3} was assumed for the calculation.

Since the presence of the undoped i-layer makes the overall depletion width of a PiN junction larger than a similarly doped PN junction (Figure 2.15), one would naturally expect a corresponding increase in the generation width W_G. Figure 2.19 compares the generation occurring at 0.5 V reverse bias between a PN junction and a PiN junction with an i-layer thickness of 300Å. Like Figure 2.18 this simulation used a full band structure plugged into (2.13), but field-enhanced generation is ignored by taking the carrier lifetimes τ_{nB} and τ_{pP} to be constant. The effective generation width is slightly wider for the PiN junction, but the difference is less than a factor of two. It thus seems reasonable that the thermal generation current of a PiN junction can be approximated to first order by the same thermal generation theory that was presented in Section 2.2, at least for the sub-2V applied biases and sub-500Å i-layer thicknesses employed in this work.

Exhaustive calculations like those in Figures 2.18 and 2.19 could be carried out for various dopings, i-layer thicknesses, and dominant generation center energies. Though mildly interesting, these calculations amount to little more than chasing down second-order effects. Because the field-enhanced emission theory given in Section 2.4.1 greatly overestimates the actual effect, inclusion of (2.43) in a full-blown simulation of (2.13) does not yield meaningful quantitative results that can be matched by experimental measurements.

Despite the inability to reach accurate quantitative conclusions concerning bulk field-enhanced emission, this mechanism is responsible for major storage time performance differences between heavily-doped experimental PN and PiN junctions. The measured data presented in Section 2.7 shows that the small increase in W_G is more than offset by the significant reduction in electric field that cuts bulk field-enhanced generation.

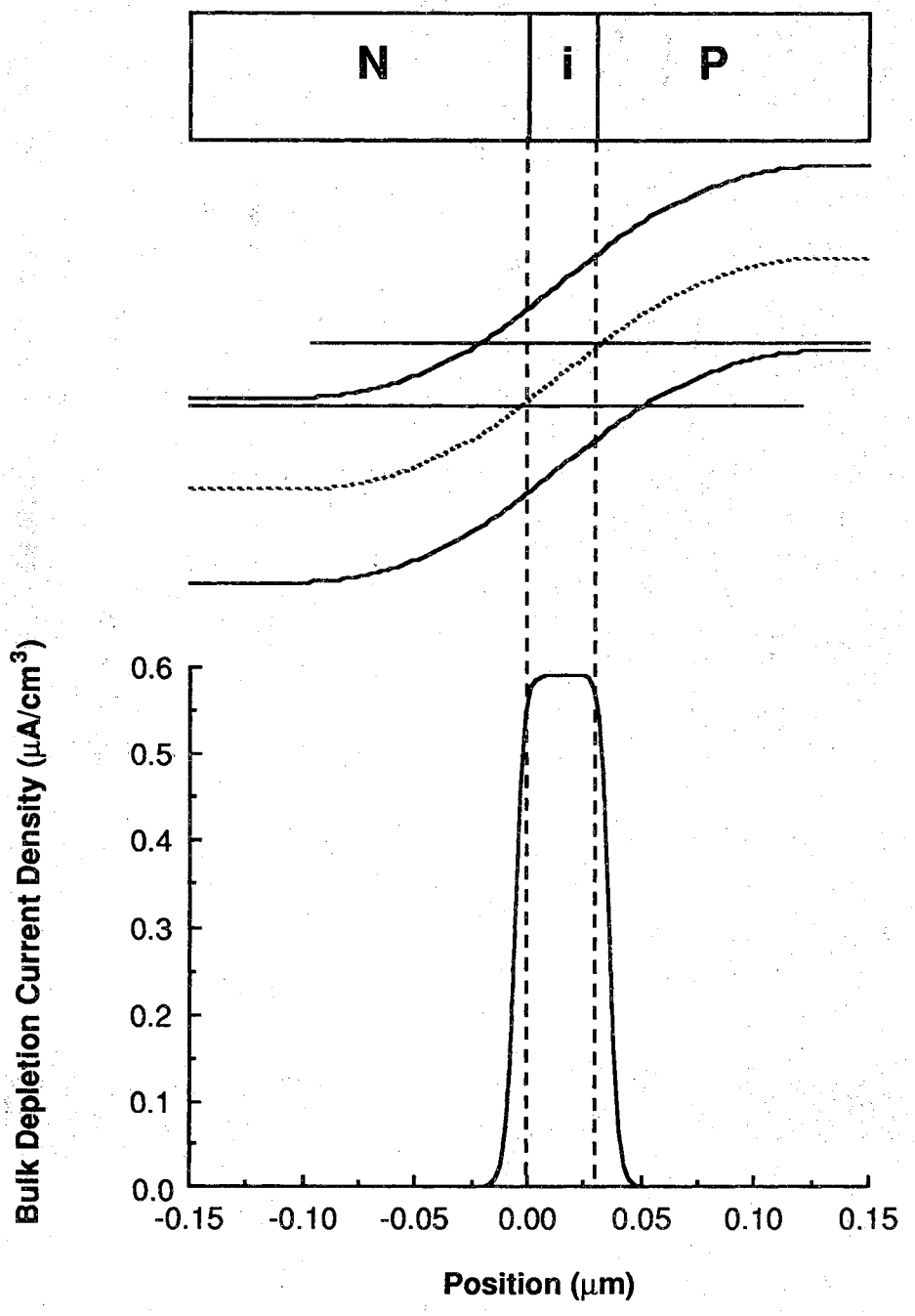


Figure 2.18 Simulated bulk generation current in a PiN junction. The curve represents a full evaluation of (2.13) neglecting field-enhanced generation. The parameters are $N_A = N_D = 10^{17}$ cm^{-3}, $x_i = 300$ Å, $V_R = 0.5$ V, and $\tau_{nB} = \tau_{pB} = 10^{-7}$ sec.

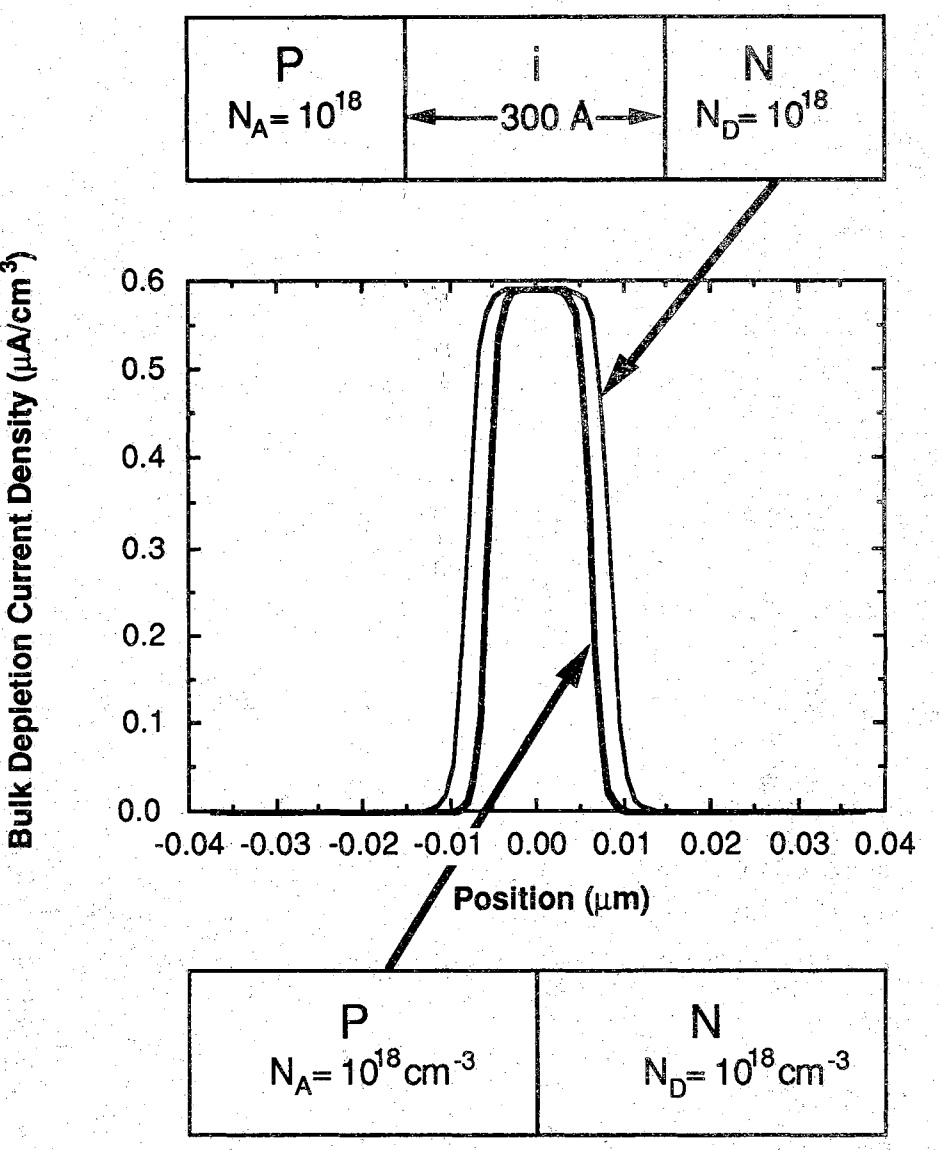


Figure 2.19 Comparison of simulated bulk generation between a PN and PiN junction. The curve represents a full evaluation of (2.13) neglecting field-enhanced generation. The calculation parameters are $V_R = 0.5$ V, and $\tau_{nB} = \tau_{pB} = 10^{-7}$ sec.

2.5.3 Theoretical PiNiP Capacitor Performance

The derivation of PiNiP storage capacitor theory is completely analogous to the PNP storage capacitor theory outlined in Sections 2.2 and 2.3, except that PN junction physics must be replaced with PiN junction physics. Careful observation of Figures 2.16 and 2.20 reveals the nature of the PiN junction capacitor design trade-off. One must choose dopings and i-layer thicknesses to maximize charge densities while keeping the built-in fields low enough that field-enhanced generation does lead to excess leakage that will kill capacitor storage times.

Like the PNP case, the charge in the capacitor is given by the number of majority carriers absent from the positive N-layer:

$$Q = 2qA\left(\frac{N_D N_A}{N_D + N_A}\right)(W' - W'_0) \tag{2.61}$$

where W'_0 is the doped-region depletion width W' defined in (2.47) at $V_A = 0$. Figure 2.20 shows the theoretical charge density of a P^+iNiP^+ structure as a function of i-layer thickness at an N-layer bias of +1 V. The decrease in charge density with i-layer thickness arises from the fact that some of the applied voltage is dropped across the undoped region, and this drop does not extract any majority carriers to contribute to capacitor charge. Expression (2.9) which relates measured PNP capacitance with stored charge is also valid for PiNiP capacitors, as can be witnessed by the combination of (2.8), (2.48), and (2.61).

As discussed in the previous section, the leakage of the PiN junctions can be approximated to first order by the PN junction leakage theory of Section 2.2. The effective generation width is thus approximated to first order by (2.21), which can be re-written using (2.48) as:

$$W_G \cong W - W_0 = W' - W'_0 \tag{2.62}$$

Substitution of (2.62) into (2.61) leads to:

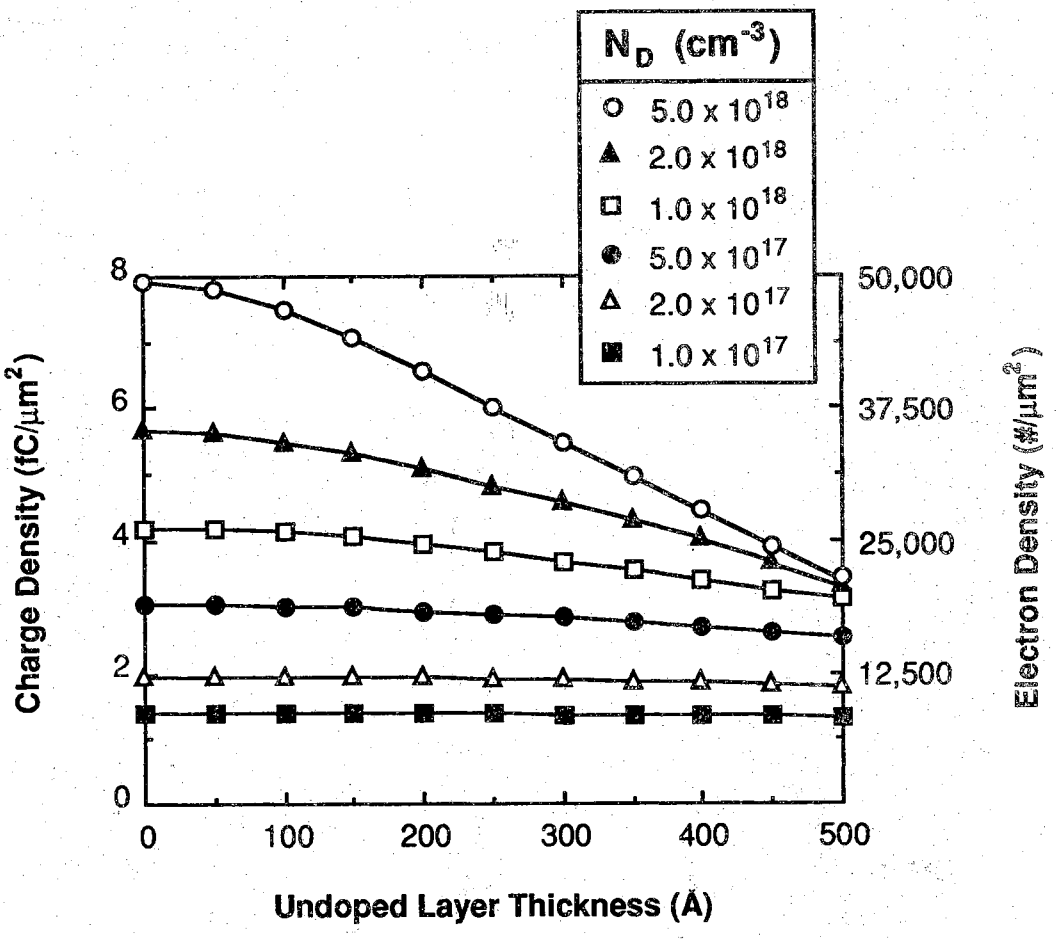


Figure 2.20 PiNiP capacitor charge storage density as a function of doping and i-layer thickness. The calculation was carried out assuming a 0 to 1V logic swing on the N-region and a P-layer doping of $N_A = 2.0 \times 10^{19}$ cm^{-3}.

$$Q = 2qA\left(\frac{N_D N_A}{N_D + N_A}\right) W_G \qquad (2.63)$$

which simplifies exactly to (2.25) for the case where $N_A >> N_D$.

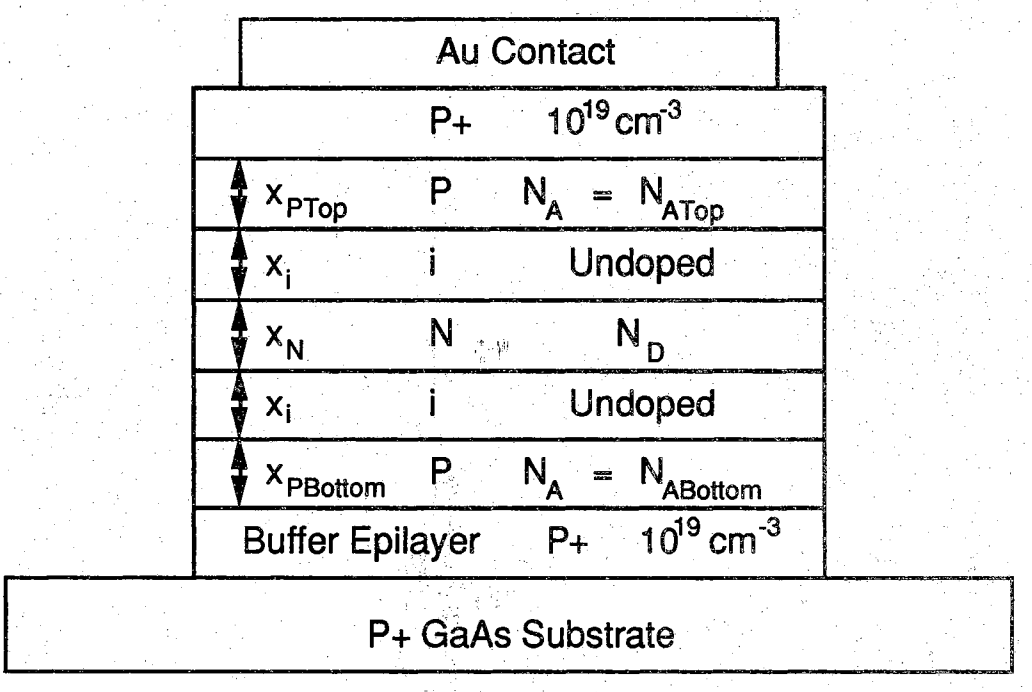
The approximations for PiNiP capacitor charge and leakage are the same as for the PNP capacitor. It therefore follows that the first order PNP storage time transient theory of Section 2.3.1 also applies to the PiNiP capacitors investigated in this work. The only significant difference manifests itself in the apparent bulk generation rate G_B via field-enhanced generation. Again, this effect is documented experimentally in Section 2.7.

2.6 Experimental PNP Capacitor Procedures

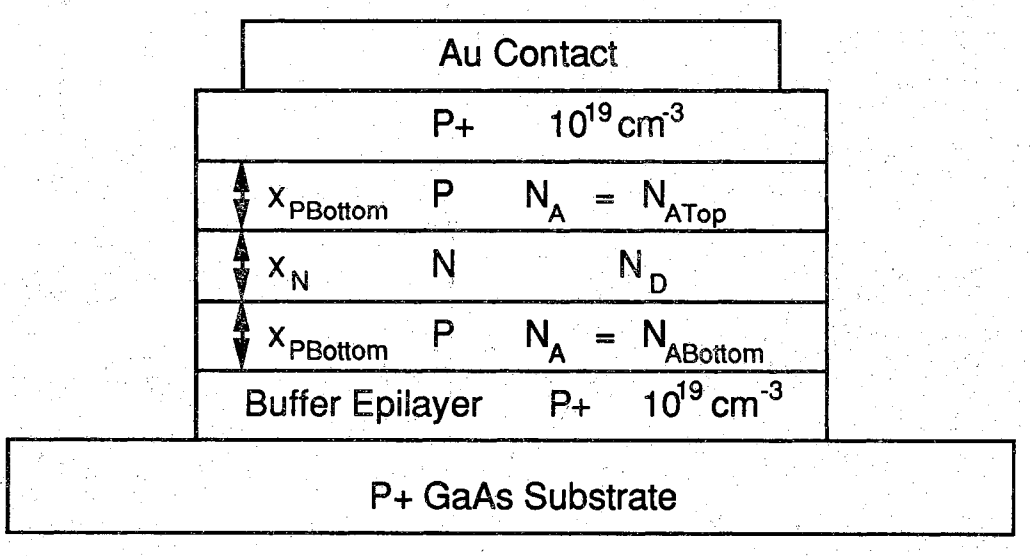
Now that a theoretical basis has been laid down in the previous sections, a thorough experimental investigation of GaAs PNP capacitors is in order. This section outlines the procedures used to conduct experimental studies on PNP and PiNiP capacitor structures.

2.6.1 Capacitor Fabrication

Most of the PN junction storage capacitors presented in this work were of the mesa-isolated epilayer variety shown in Figure 2.21. As many runs with differing layer dopings and thicknesses were carried out, only the generalities of PNP and PiNiP device fabrication are discussed here. Runsheets outlining specific fabrication procedures are given in the Appendices. A highly conductive P^+ (100)-oriented GaAs substrate was used as the starting material. All growths started with a P^+ buffer layer ($N_A > 10^{19}$ cm^{-3}) to minimize the propagation of substrate-induced crystal defects into device active areas [15,114]. The layers were grown so that the top and bottom junctions were as similar as possible. The active N and P layer thicknesses x_P an x_N were designed so that they were never entirely depleted at junction biases of less than 2 V. All growths were capped with P^+ layers to facilitate highly conductive non-alloyed contacts to the top of



a.) PiNiP Capacitor



b.) PNP Capacitor

Figure 2.21 Experimental PNP and PiNiP capacitor structures.

the device. Metal contacts to the top of the capacitors are evaporated and patterned by liftoff in the first masking step. Fabrication is concluded by the second mask step, a patterned wet etch to define the mesas. To insure good electrical contact to the substrate during characterization, capacitor wafers were mounted onto a mechanical substrate using either indium or a conductive paint.

2.6.2 Electrical Measurement of Storage Time

As outlined in Section 2.1.3, experimental observation of charge decay was accomplished by measuring the device capacitance. Storage time measurements were conducted on the apparatus pictured in Figure 2.22. A MicroManipulator probe station inside a shielded dark-box was used to contact the devices, and all storage time measurements were carried out in the dark. A hot-chuck with built-in heating element and J-type thermocouple was used to perform high temperature device characterization. A Boonton 72B meter was used to monitor device capacitance, and data from the meter's analog output was recorded on a Tektronix 11401 digitizing oscilloscope. Manually triggered single-shot pulses were fed to the device via the capacitance meter bias inputs. In most cases the pulse height was 1-V.

Figure 2.6 was constructed using actual storage time measurement waveforms. The top trace is the applied voltage pulse, while the bottom waveform is the response of the capacitance meter. As discussed in Section 2.1, charge is written to the capacitor by the positive bias pulse, and the return of the device to equilibrium is monitored through the capacitance. With the device carrying its largest charge at $t = 0^+$, the capacitance takes on its minimum value $C_{PNP}(0)$. As the device charge decays, the measured capacitance C_{PNP} correspondingly increases until it is restored to its zero-charge equilibrium value C_{PNP0}. Using (2.9) it is possible to calculate charge from the measured capacitance, and that data in turn could be logarithmically fit to (2.30) to produce an accurate exponential time constant.

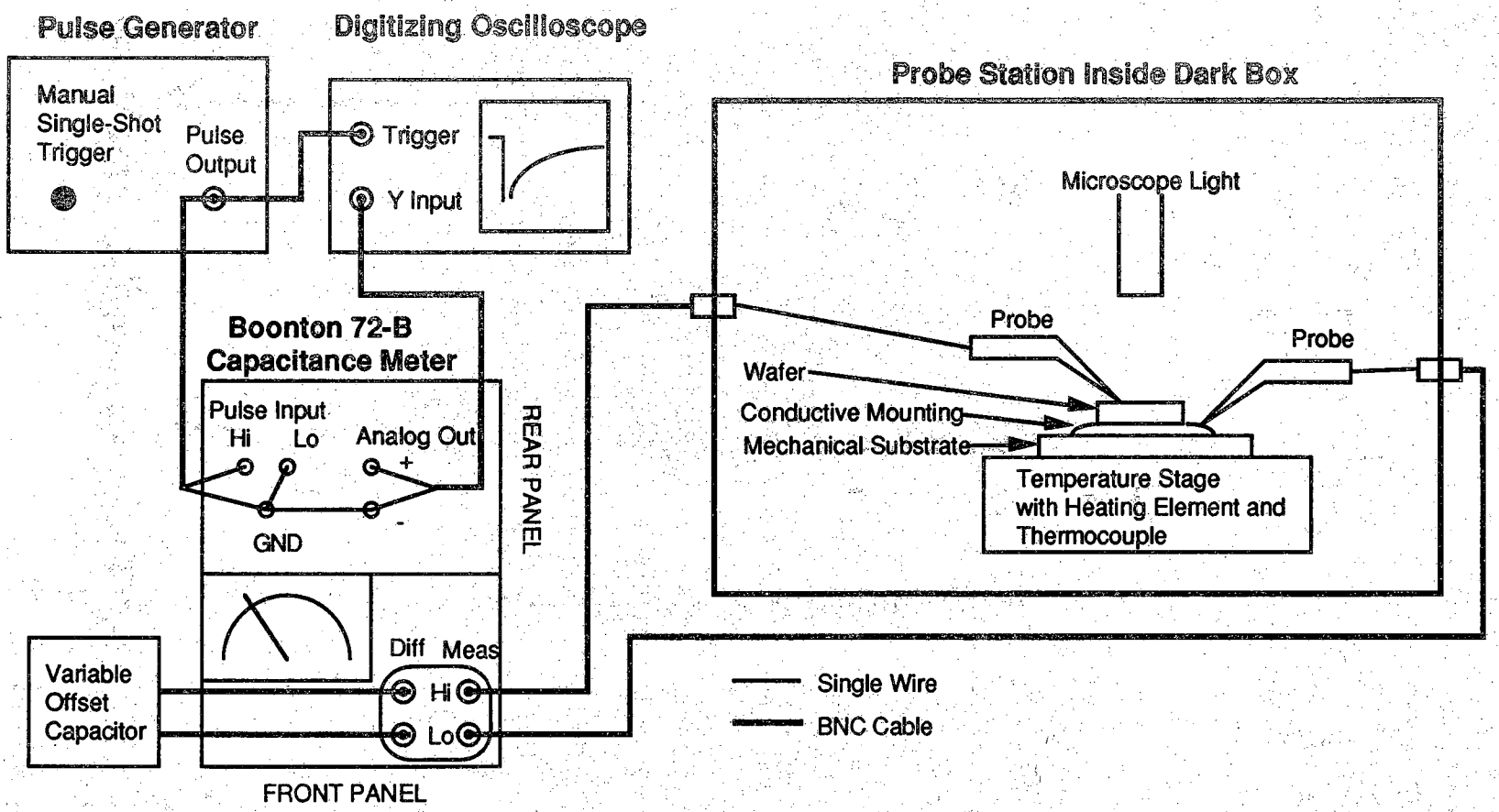


Figure 2.22 Schematic representation of experimental apparatus used to conduct PNP capacitor storage time measurements.

is made throughout the rest of this dissertation. Section 2.7.1 demonstrates the experimental validity of this assertion in detail.

2.7 PNP Capacitor Experimental Results

Previous sections of this chapter described the general theory of PN junction storage capacitors. This section summarizes the experimental data collected on PNP storage capacitors to date. This data supports most of the general arguments presented in Sections 2.3, and an effort is made to correlate physical theory with experimental observations. Although most of the text is focused on physical device phenomena one should not lose sight of the key result of these experiments, namely that PN junction capacitor storage times are long enough for use in a practical GaAs DRAM.

2.7.1 Verification of Storage Time Measurement

This section demonstrates the validity of the first-order exponential storage time approximation (2.30) for a PiNiP storage capacitor structure. An ALE-grown PiNiP capacitor ($N_A > 10^{19}$ cm^{-3}, $N_D = 10^{17}$ cm^{-3}, $x_i = 310$ Å, and A = 140 x 160 μm^2) yielded the room-temperature storage time transients of Figure 2.23. The upper trace is the measured capacitance transient $C_{PNP}(t)$, while the lower trace is the calculated charge transient Q(t) obtained by plugging measured capacitance data into (2.9). The time constants found by locating the 1/e decay point on the two curves differ by less than 5%.

The exponential behavior of the charge and capacitance recovery transients can be checked by plotting their normalized values on a logarithmic scale. As the charge in (2.30) follows a simple exponential behavior, so will the normalized charge $Q_{Norm}(t)$:

$$Q_{Norm}(t) = \frac{Q(t)}{Q(0)} = e^{-t/\tau_s} \tag{2.68}$$

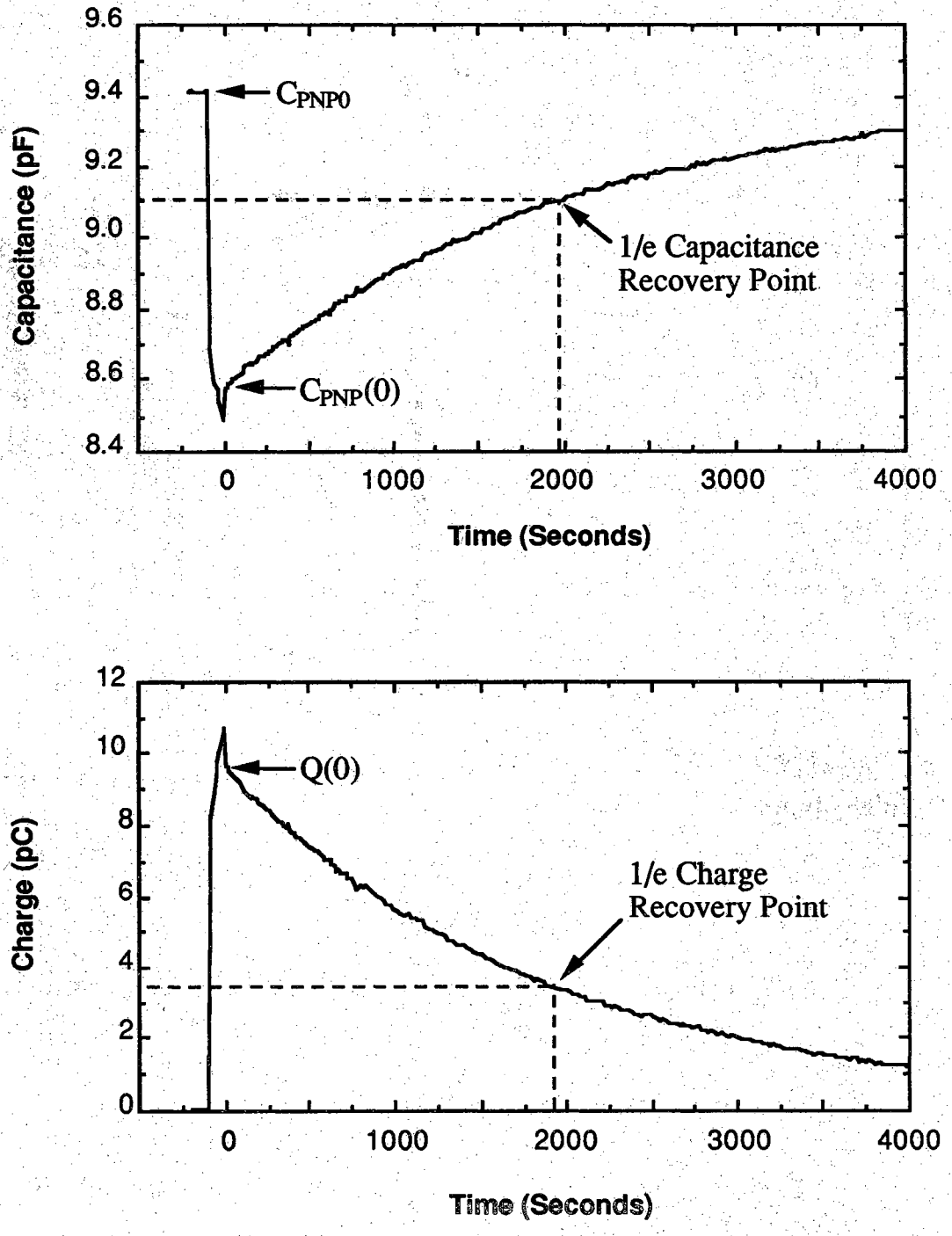


Figure 2.23 PiNiP device capacitance and charge recovery transients. The 1/e capacitance recovery occurs at t = 1982 seconds, while the 1/e charge recovery occurs at t = 1890 seconds.

By defining the normalized capacitance $C_{PNPNorm}$ as:

$$C_{PNPNorm} = \frac{C_{PNP}(t) - C_{PNP}(0)}{C_{PNP0} - C_{PNP}(0)} \qquad (2.69)$$

$1 - C_{PNPNorm}$ will have a simple exponential behavior:

$$1 - C_{PNPNorm} = e^{-t/\tau_C} \qquad (2.70)$$

If the charge and capacitance transients are truly exponential, then (2.68) and (2.70) imply that logarithmic plots of $Q_{Norm}(t)$ and $1 - C_{PNPNorm}(t)$ will be linear, and the inverse slope will yield the exponential time constants.

Figure 2.24 shows the logarithmic plots of $Q_{Norm}(t)$ and $1 - C_{PNPNorm}(t)$ for the recovery transients of Figure 2.23. The exponential behavior predicted by first-order storage time theory (Section 2.3.1) is illustrated by the high linearity of the plots. The storage time constants extracted from the slopes not only fall within 5% of each other, but are also within 5% of the time constants calculated from the 1/e recovery points in Figure 2.23. The simplified storage time measurement procedure described in Section 2.6.2 thus appears to be justified, and in particular the assumption that $\tau_S = \tau_C$ seems valid. The exponential nature of the charge recovery suggests that the first-order approximations of Sections 2.2, 2.3, and 2.4 apply quite well to actual devices.

2.7.2 The Light-Off Transient

The accurate measurement of the zero-charge equilibrium capacitance C_{PNP0} is vital to the determination of the 1/e capacitance decay point. However, the determination of of C_{PNP0} is non-trivial in capacitors with long storage times, due to the fact that it takes a considerable amount of time for a perturbed device to return to equilibrium. Excess carriers generated by light from the microscope during probe manipulations put the capacitor in a negatively charged state with the PN junctions slightly

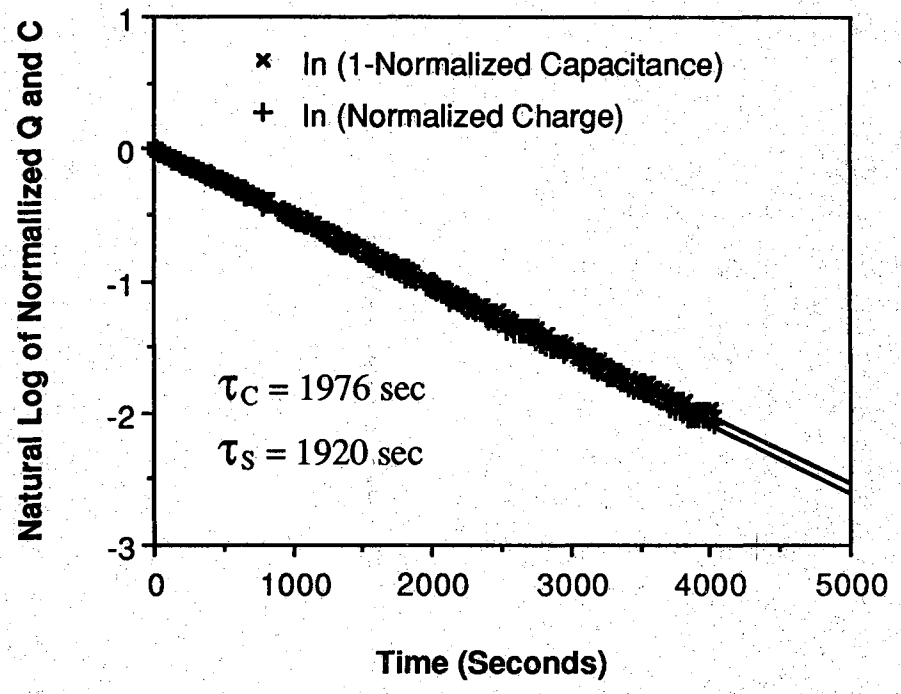


Figure 2.24 PiNiP normalized capacitance and charge on a logarithmic scale versus time. The linearity demonstrates the exponential behavior of the recovery transients, and the difference between the time constants calculated from the slopes is less than 5%.

forward biased. At low N-region voltages the forward current is small enough that it takes a considerable amount of time for the device to return to equilibrium after the light has been turned off. This phenomenon is referred to as the light-off transient. Exact measurements have not been conducted, but a general experimental observation is that light-off transient decay times are in the general neighborhood of capacitor storage times. Figure 2.25 shows the light-off transient taken from the PiNiP device of Section 2.7.1.

2.7.3 Experimental Scaling Dependence

The storage time expressions derived in Section 2.3 imply that τ_S will scale with the device perimeter-to-area. The scaling phenomenon is observed experimentally by applying (2.34) to plots of $1/\tau_S$ versus P/A. Figure 2.26 shows the 130 °C scaling behavior of capacitors fabricated from an MBE-grown $P^+iN^+iP^+$ film ($N_A > 10^{19}$ cm^{-3}, $N_D = 10^{18}$ cm^{-3}, x_i = 300Å). Consistent with the arguments presented in Section 2.3.2, the storage times decrease as device sizes shrink due to the increasing P/A ratio. The non-zero slope demonstrates via (2.34) that perimeter generation plays a non-trivial role in the storage time performance of devices on this wafer. Furthermore the non-zero y-intercept indicates that bulk generation is also significant, as the maximum bulk-limited 130 °C storage time for this film is about two seconds.

An alternative method of documenting the scaling behavior is suggested by (2.36), which inversely relates the storage time τ_S of a PNP capacitor to the reverse leakage current density J_R of its PN junctions. By measuring the current density of diodes under the appropriate reverse bias, (2.36) or (2.39) can be used to roughly predict device storage times of analogous PNP capacitor structures. Given no major differences in material quality, this rough approximation is valid as long as the voltage at which the diode current density is measured is similar to the potential that the capacitor N-region is charged to by a bias pulse. Of course the scaling dependence dictates that devices of like perimeter-to-area ratios be

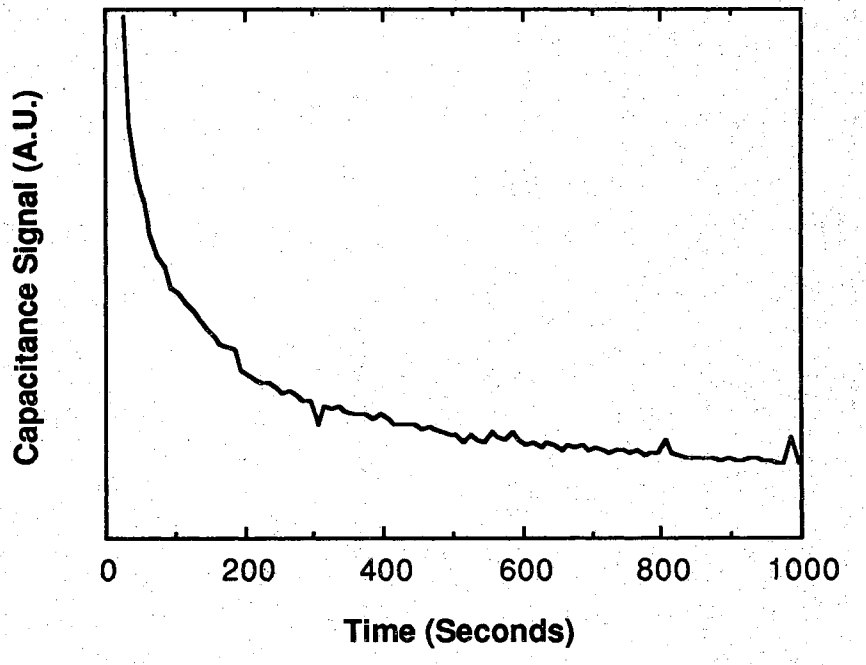


Figure 2.25 Light-off transient of a PiNiP storage capacitor. The light is turned off around t = 0, but after 1000 seconds the device hasn't returned to equilibrium.

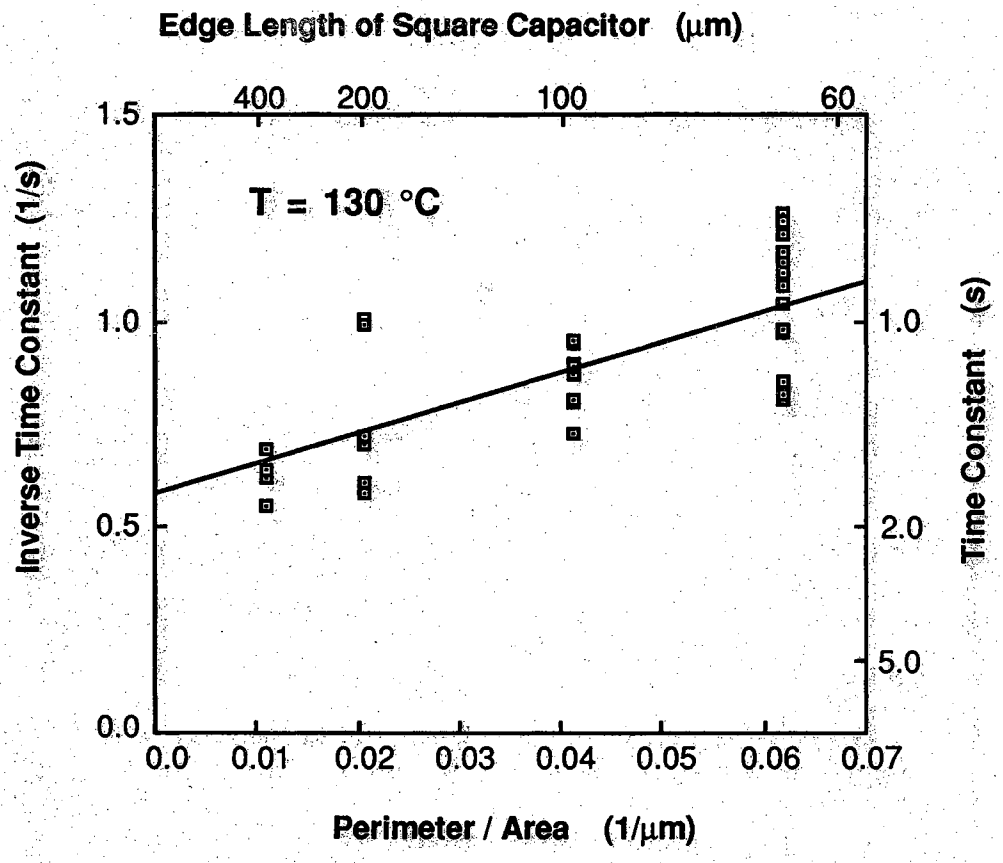


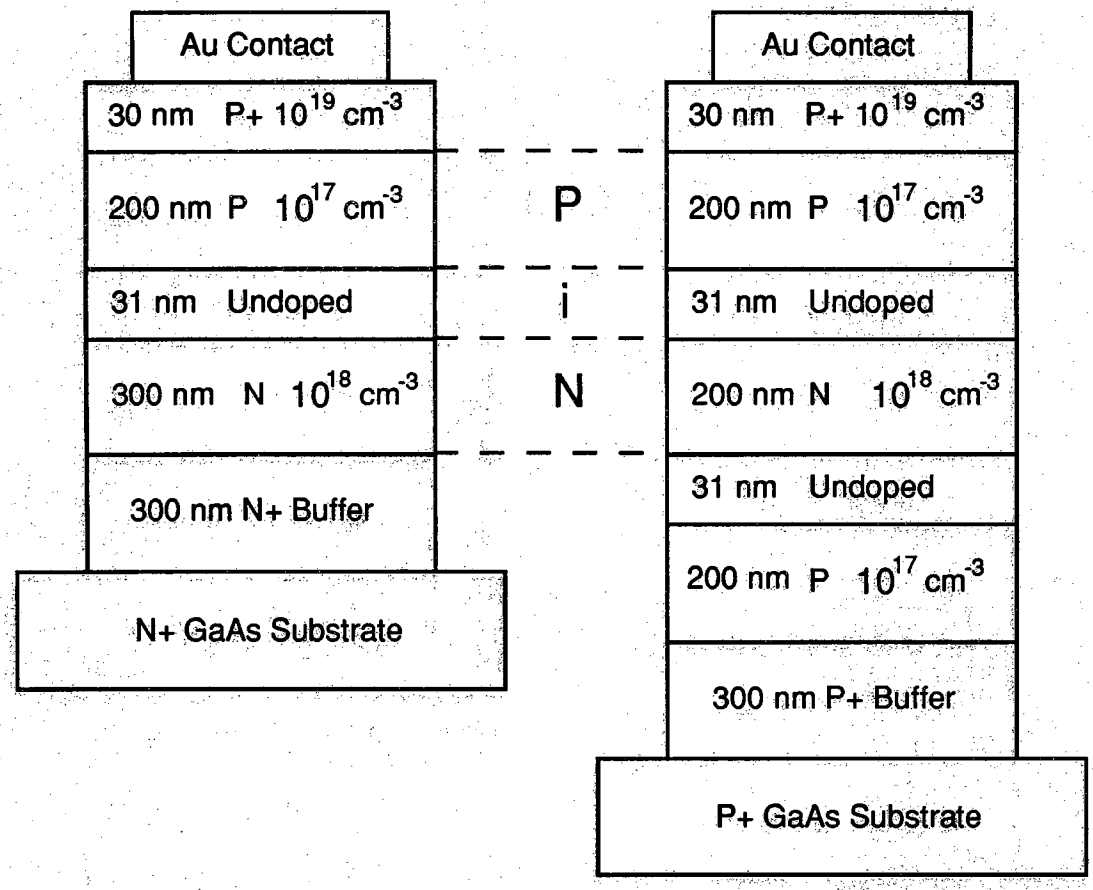
Figure 2.26 Storage time performance of $P^+iN^+iP^+$ capacitors versus perimeter-to-area ratio. This plot shows that both bulk generation and perimeter edge generation are significant leakage mechanisms limiting capacitor storage time. Parameters: $N_A > 10^{19}$ cm^{-3}, $N_D = 10^{18}$ cm^{-3}, and $x_i = 300$Å. After References [1] and [2].

compared. It is important to note that junction leakages cannot be ascertained through picoammeter measurements of PNP structures, due to the fact that parasitic bipolar action will amplify the current. (The measurement would correspond to a measurement of $I_{CEO} \cong I_{CBO}(\beta_{DC} + 1)$ on a bipolar transistor [119]).

Current and storage time measurements were carried out on the analogous PiN^+ diode and PiN^+iP capacitor structures shown in Figure 2.27. The PiN^+ diode reverse leakage currents were too small for measurement with a picoammeter at room temperature, so characterization was conducted at temperatures above 110 °C. Table 2.1 compares measured PiN^+iP storage times (τ_{SMeas}) with storage times calculated (τ_{SCalc}) by inserting PiN^+ diode current densities measured at 1V reverse bias ($J_{Meas}(-1V)$) into (2.36). It should be noted that the ALE-grown capacitor wafer (Figure 2.27b) was plagued with visible point defects resulting in very few working devices. It is believed that large differences between τ_{SMeas} and τ_{SCalc} are due to undetected point defects in the capacitors.

Figure 2.28 shows the scaling dependence of PiN^+ diodes under 1 V reverse bias at three different temperatures. The measured bulk generation current J_{BG} is very small compared to the perimeter generation current J_{PG}, as evidenced by the very small y-intercepts. Corresponding PiNiP storage capacitors thus fall into the perimeter-dominated category at these temperatures, with the storage time effectively given by (2.33).

It is useful to compare the storage time performance of the two capacitor cross-sections mentioned above, the $P^+iN^+iP^+$ structure of Figure 2.26 and the PiN^+iP capacitor of Figure 2.27b. Given comparable P/A ratios at 130 °C, the storage times are consistently longer for the $P^+iN^+iP^+$ devices (Figure 2.26) than for the PiN^+iP devices (Table 2.1). However, one can not immediately conclude from this that the generation rates G_B and G_P are less in the heavier-doped device because the generation width W_G is different for the two structures. Table 2.2 compares the apparent bulk and perimeter generation rates extracted from the application of (2.34) to Figure 2.26 and (2.21) and (2.35) to Figure 2.28.



a) PiN^{+} Diode b) $PiN^{+}iP$ Capacitor

Figure 2.27 Cross-sections of analogous ALE-grown PiN^{+} diode and $PiN^{+}iP$ capacitor structures.

Table 2.1 Comparison of measured diode leakage current densities to theoretical and measured capacitor storage times. The ALE-grown capacitor wafer was plagued with visible point defects resulting in a very low device yield. Some differences between τ_{SMeas} and τ_{SCalc} are believed to be due to undetected point defects in the capacitors.

Device P/A Ratio (1/μm)	Temperature (°C)	PiN⁺ Diode $J_{Meas}(-1V)$ ($\mu A/cm^2$)	Calculated PiN⁺iP τ_{SCalc} (seconds)	Measured PiN⁺iP τ_{SMeas} (seconds)	$\frac{\tau_{SMeas}}{\tau_{SCalc}}$
0.04	145	1.02	0.0069	0.0063	0.91
0.04	130	0.450	0.158	0.150	0.95
0.04	114	0.141	0.503	0.25	0.50
0.0343	145	0.871	0.814	0.120	0.15
0.0343	130	0.350	0.203	0.290	1.42
0.0343	114	0.104	0.682	0.780	1.14
0.0268	145	0.679	0.104	0.235	2.26
0.0268	130	0.257	0.276	0.550	1.99
0.0268	114	0.0665	1.07	1.40	1.31

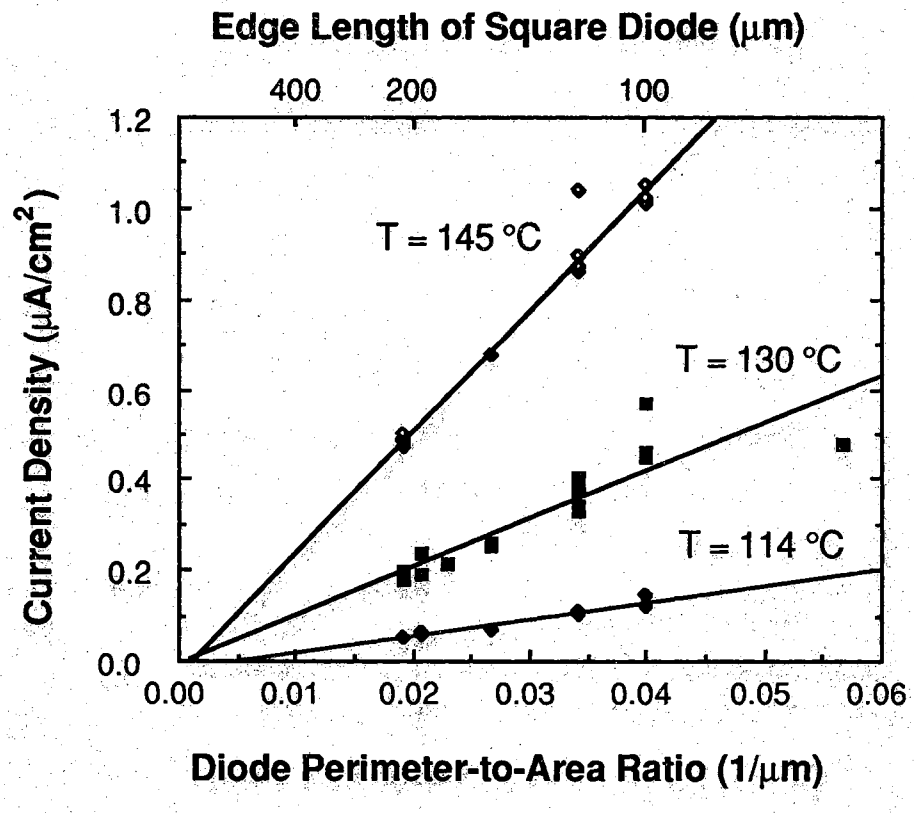


Figure 2.28 Dependence of current density on device perimeter-to-area ratio at 1-V reverse bias for the ALE-grown PiN$^+$ diode structure of Figure 2.27a. The very small y-intercept for these devices indicates that generation current in the bulk ALE-grown material is small compared to generation current from the etched perimeter.

Table 2.2 Comparison of Bulk and Perimeter Generation in $P^+iN^+iP^+$ and PiN^+iP Storage Capacitors.

Device	N_A (cm^{-3})	N_D (cm^{-3})	x_i (Å)	W_G(-1V) (Å)	G_P ($cm^{-2}\,sec^{-1}$)	G_B ($cm^{-3}\,sec^{-1}$)
$P^+iN^+iP^+$	10^{19}	10^{18}	300	126	7.5×10^{14}	5.8×10^{17}
PiN^+iP	10^{17}	10^{18}	310	443	1.5×10^{15}	$< 7.0 \times 10^{16}$

The factor of two difference in perimeter generation rate may be due to the fact that the mesa perimeters were defined with different etchants affecting the surface state distribution and surface recombination velocity [15,120]. Of much greater consequence however is the difference in the observed bulk generation rates, which is probably greater than an order of magnitude. At first inspection one might carelessly attribute the difference in G_B to a difference in the number of bulk defects unintentionally incorporated during material growth, especially in light of the fact that the $P^+iN^+iP^+$ film was grown by MBE while the PiN^+iP film was ALE-grown. However, a more careful analysis of the situation reveals that the field-enhanced generation phenomenon presented in Section 2.4.1 is probably responsible.

Table 2.3 summarizes calculations performed to back the assertion that field-enhanced emission could be responsible for the experimentally observed difference in G_B. Despite the presence of the i-layer to reduce built-in fields, the peak electric field of the $P^+iN^+iP^+$ device is more than twice that of the PiN^+iP device. The theoretical barrier lowering ΔE due to the built-in field is calculated using Frenkel's theory is given in (2.42), and the thermionic emission model is used to calculate a generation rate enhancement factor $e^{\Delta E/kT}$. The difference between the theoretical rate enhancement factors is large enough to account for the difference in measured bulk generation rate.

Table 2.3 Comparison of measured G_B with theoretical field barrier lowering.

Device	G_B (cm^{-3} sec^{-1})	ε'_{Peak}(0V) (kV/cm)	ΔE (eV)	$e^{\Delta E/kT}$
$P^+iN^+iP^+$	5.8×10^{17}	336	0.243	1100
PiN^+iP	$< 7.0 \times 10^{16}$	158	0.166	120

2.7.4 Experimental Temperature Performance

In addition to providing an idea of the temperature range over which a GaAs DRAM might be capable of operating, the temperature performance of PNP capacitors provides valuable insight into the physical leakage mechanisms that govern device storage time. The temperature performance of τ_S in (2.31) is specified by the temperature dependence of the generation rates G_B and G_P. The simplified generation rates (which were calculated assuming midgap generation centers) given in (2.23) and (2.19) are proportional to the intrinsic carrier concentration, and n_i in turn is exponentially dependent on the bandgap E_G. Other diode variables like V_{bi} have some temperature dependence, but their effect on the temperature performance of leakage current is negligible. The intrinsic carrier concentration is given by [54,56]:

$$n_i = \sqrt{N_C(T)N_V(T)}\, e^{-E_G(T)/2kT} \qquad (2.71)$$

The variation of the effective density of states N_C and N_V with temperature:

$$\sqrt{N_C(T)N_V(T)} = \sqrt{N_C(0)N_V(0)}\, T^{3/2} \qquad (2.72)$$

is small compared to the exponential term of (2.71) [54,56].

If E_G were constant, the storage time would scale exponentially with temperature, and a measurement of the storage time activation energy would yield $E_G/2$ [121]. However, the GaAs bandgap varies with temperature according to [122]:

$$E_G(T) = 1.519 - \frac{5.405 \times 10^{-4} T^2}{T + 204} \text{ eV} \qquad (2.73)$$

For the temperature range of experimental interest (300 K < T < 450 K), (2.73) approximates to a linear relationship:

$$E_G(T) = E_{GE0} - \alpha T \text{ eV} \qquad (2.74)$$

As depicted in Figure 2.29, E_{GE0} is the zero-temperature intercept of the linear approximation of $E_G(T)$. E_{GE0} = 1.58 eV and $\alpha = 5.405 \times 10^{-4}$ eV/K applies to GaAs in the experimental temperature range of interest. The substitution of (2.74) into (2.71) yields:

$$n_i = \left(\sqrt{N_C N_V}\, e^{-\alpha/2k}\right) e^{-E_{GE0}/2kT} \qquad (2.75)$$

This approximation suggests the intrinsic carrier concentration should exhibit a thermal activation energy near half the extrapolated zero-temperature bandgap.

Figure 2.30 shows activation energy plots of n_i arrived at through three calculation methods. The simulation calculated with the full temperature dependence of all variables via (2.71), (2.72), and (2.73) yields a measured activation energy of 0.83 eV. A second calculation that included (2.71) and (2.73) but ignored the temperature variation of the density of states in (2.72) produced an apparent activation energy of 0.78 eV. The third simulation of Figure 2.30 is based entirely on the approximate relations (2.74) and (2.75), so it naturally yields an activation energy of $E_{GE0}/2$ = 0.79 eV.

The experimental temperature performance of low-built-in-field (i.e., lightly-doped) GaAs PN and PiN device structures correlates well

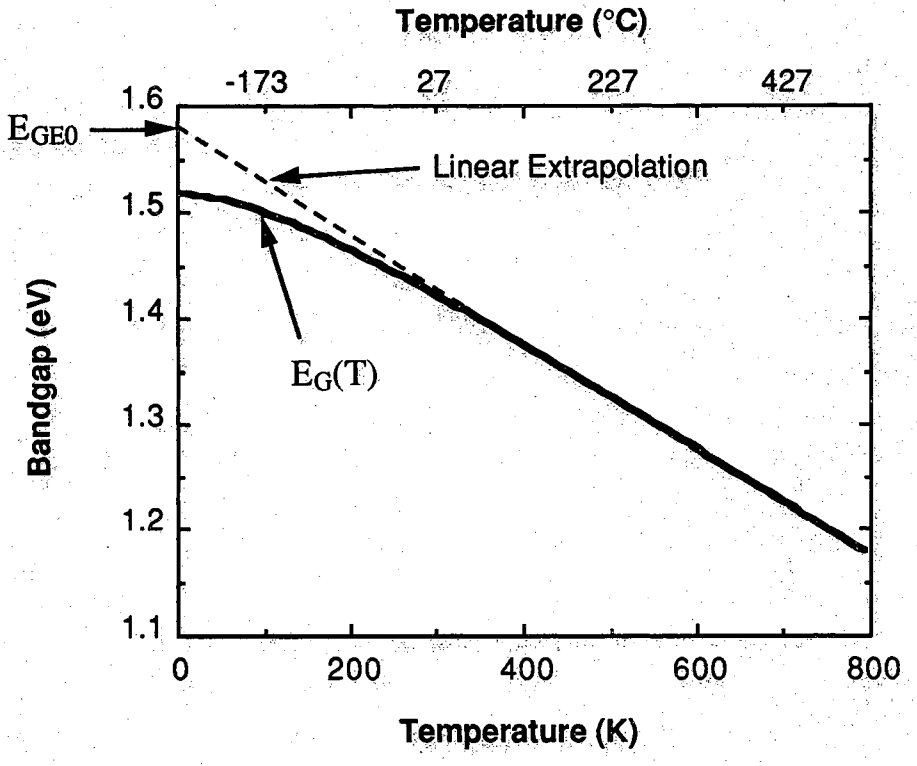
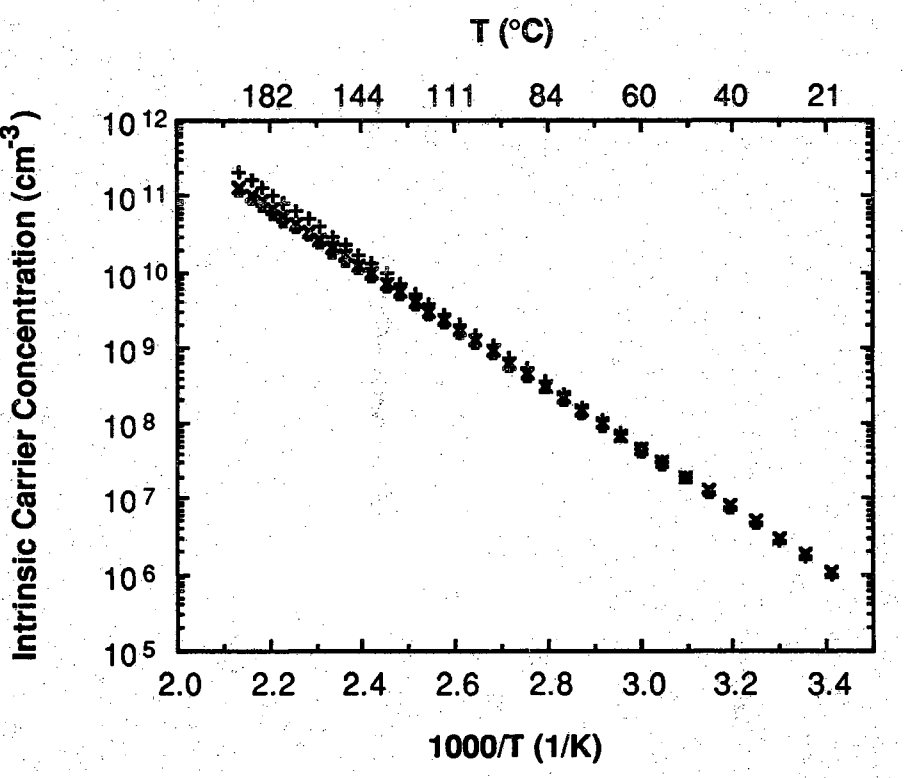


Figure 2.29 Variation of GaAs bandgap with temperature. The solid line is the relationship given by (2.73), while the dotted line represents the linear extrapolation of (2.74).



+ Full Temperature Dependence, E_A = 0.830 eV
▪ Neglecting Density of States Temperature Dependence, E_A = 0.782 eV
× Linear Bandgap Approximation, E_A = 0.790 eV

Figure 2.30 Activation energy plots of n_i arrived at through three calculation methods.

with the temperature dependence of n_i discussed above [1,2,4,5,10,11]. Figure 2.31 shows the storage time activation energy plots of the two low-built-in-field capacitor structures investigated in this work. Activation energies obtained from best-fit lines are close to half the extrapolated zero-temperature bandgap of 0.79 eV, and this corresponds to work reported elsewhere [14]. These experimental results support the hypothesis that near-midgap centers are controlling generation in high-quality reverse-biased GaAs PN junctions.

Figure 2.32 shows the storage time activation energy plots of capacitors with higher built-in fields. These samples exhibit markedly lower activation energies than their lighter-doped counterparts. The experimental evidence gathered to date suggests that field-enhanced bulk generation is responsible. Despite the fact that storage times are influenced by perimeter generation, Table 2.4 exhibits a trend of decreasing activation energy with increasing peak electric field. This trend is qualitatively consistent with the field-enhanced bulk generation phenomenon presented in Section 2.4.1, as the barrier lowering will lead to lower bulk activation energies.

A closer look at the $P^+N^+P^+$ device of Figure 2.32 reveals a difference in slope between high and low temperatures. Two best-fit lines could conceivably be drawn, one that is fit to high temperature data points and one that is fit to low-temperature data points. This suggests the presence of two leakage mechanisms with differing activation energies. Super-close inspection of Figure 2.32 reveals that the activation plots on all of the heavier-doped capacitors are slightly curved, with the higher slope (E_A) occurring at higher temperatures.

There is ample evidence to support the proposition that perimeter generation is the mechanism with the higher activation energy, while field-enhanced bulk generation dominates at lower temperatures. In contrast to bulk generation, previous work suggests that perimeter generation is relatively immune to field-ehancement [1]. In the case of midgap-dominated generation, this would lead G_P to exhibit a higher activation energy than G_B. The surface-dominated PiN^+iP capacitor of Section 2.7.3 exhibits an E_A of 0.79 eV. Its $P^+iN^+iP^+$ counterpart, whose bulk current component is readily visible in Figure 2.26, shows a lower E_A of 0.63 eV.

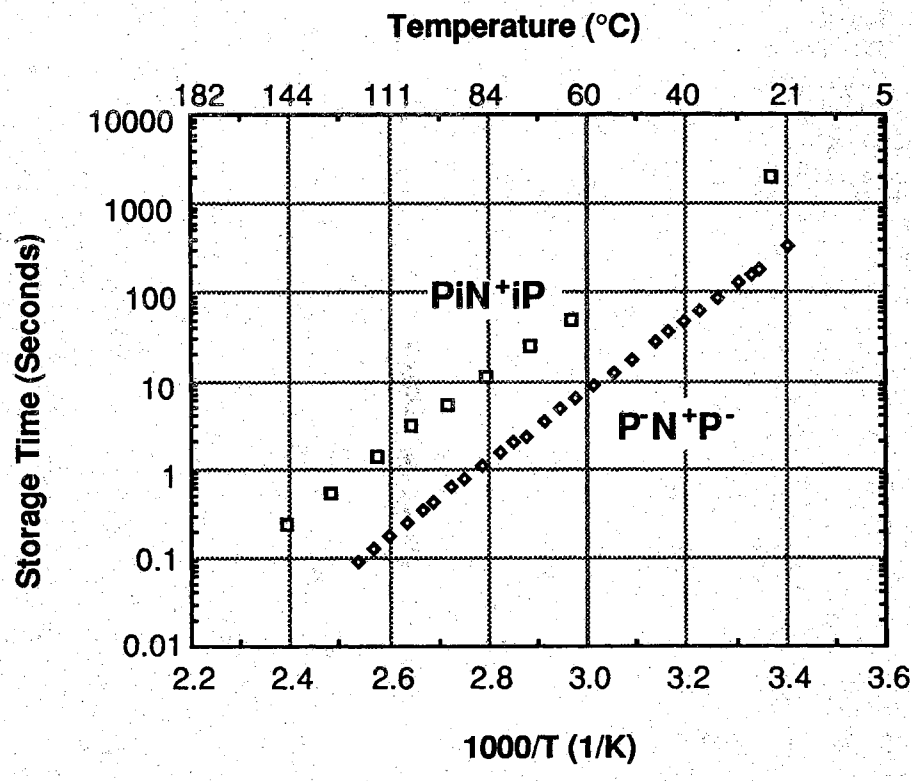


Figure 2.31 Storage time versus temperature performance of low-built-in-field junction capacitors. The activation energy of the PiN^+iP sample ($N_A = 10^{17}$ cm^{-3}, $N_D = 10^{18}$ cm^{-3}, $x_i = 300$Å, $\varepsilon_{Peak} = 158$ kV/cm) is 0.79 eV, while the $P^-N^+P^-$ sample ($N_A = 7 \times 10^{15}$ cm^{-3}, $N_D = 1.2 \times 10^{18}$ cm^{-3}, $\varepsilon_{Peak} = 40$ kV/cm) exhibits a 0.80 eV activation energy. The $P^-N^+P^-$ device data was taken from Reference [1].

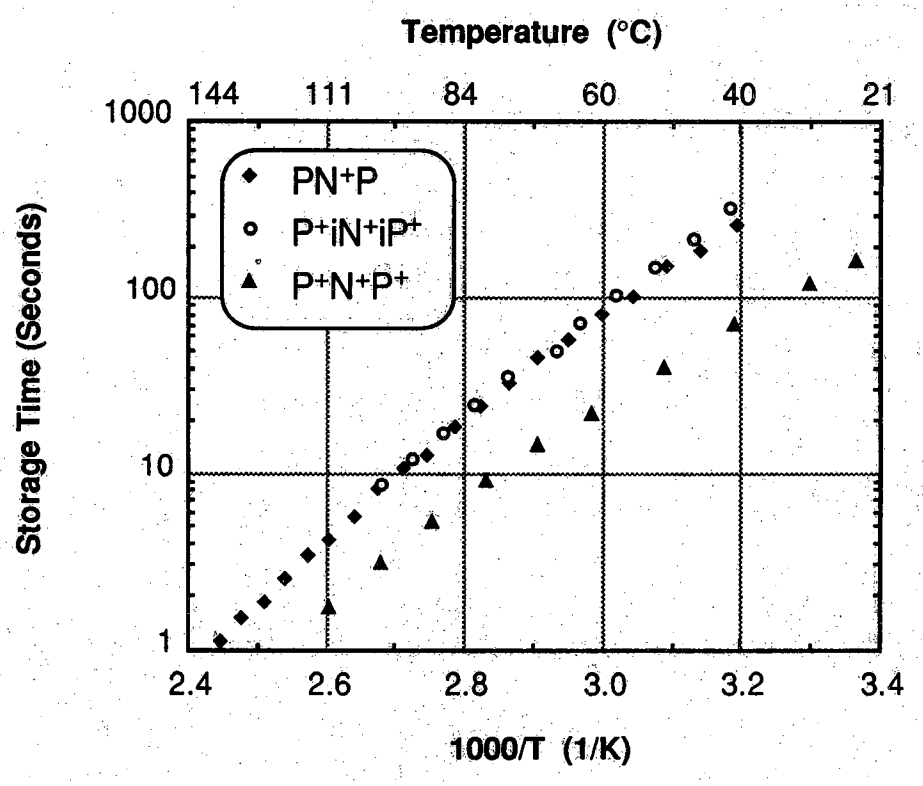


Figure 2.32 Storage time versus temperature performance of high-built-in-field junction capacitors. The activation energies for the PN^+P, $P^+iN^+iP^+$, and $P^+N^+P^+$ samples are 0.62 eV, 0.63 eV, and 0.51 eV respectively. This data was taken from Reference [1], and doping profiles and peak fields are summarized in Table 2.4.

Table 2.4 Activation energies measured on PNP and PiNiP capacitor structures. It should be noted that perimeter scaling effects have not been taken into account, but large devices that maximize the bulk component are presented.

Device	N_A (cm^{-3})	N_D (cm^{-3})	x_i (Å)	$\mathcal{E}_{Peak}$(0V) (kV/cm)	ΔE (eV)	E_A (eV)
$P^-N^+P^-$	7.0×10^{15}	1.2×10^{18}	0	40	0.083	0.80
PiN^+iP	1.0×10^{17}	1.0×10^{18}	310	158	0.166	0.79
PN^+P	1.0×10^{17}	1.0×10^{18}	0	196	0.186	0.62
$P^+iN^+iP^+$	1.0×10^{19}	1.0×10^{18}	300	336	0.243	0.63
$P^+N^+P^+$	1.0×10^{19}	1.0×10^{18}	0	605	0.326	0.51

2.7.5 Experimental Doping Profile Performance

Despite quantitative comparison difficulties, some very useful estimates and conclusions can be drawn from the measured data presented so far. First and foremost is the fact that storage times appear to increase with lighter-side junction doping as predicted by (2.31) until built-in fields cause significant field enhanced generation.

The doping dependence of (2.31) can be observed directly in the low-built-in-field samples of Figure 2.31. Given $N_A >> N_D$, like generation rates G_B and G_P, and like P/A ratios, (2.31) predicts that the ratio of storage times between the two wafers will be:

$$\frac{\tau_{S1}}{\tau_{S2}} = \frac{N_{A1}}{N_{A2}} \qquad (2.76)$$

the same as the ratio of the lighter-side dopings. The low built-in fields and half-bandgap activation (Table 2.4) in these samples suggest that field-enhanced generation is insignificant. A qualitative examination of Figure 2.13 reveals that the storage time of the heavier doped capacitor is

substantially larger as predicted by (2.31). However, an interesting numerical comparison of these two devices can be made based on a few reasonable assumptions. The devices measured for Figure 2.31 were unlike in size, so the difference in P/A ratio must be taken into account. The measurements of Section 2.7.3 demonstrated the perimeter-dominated nature of the PiN^+iP device at high temperatures (Figure 2.28), and the fact that there is no change in activation energy at low temperatures suggests that perimeter generation is dominant for the entire temperature range of Figure 2.31. It is therefore reasonable to account for the size difference by scaling the PiN^+iP device to the $P^-N^+P^-$ device's P/A ratio, and this is done in Row #3 of Table 2.5.

Table 2.5 Storage time comparison of low-built-in-field capacitor samples.

#	Device	P/A ($1/\mu m$)	N_A (cm^{-3})	τ_S (24 °C) (sec)	τ_S (74 °C) (sec)	τ_S (114 °C) (sec)
1	$P^-N^+P^-$	0.0133	7.0×10^{15}	230	2.2	0.13
2	PiN^+iP	0.0268	1.0×10^{17}	1976	25	1.4
	Ratio #2/#1	2.0	14.3	8.6	11.3	10.7
3	Adjusted PiN^+iP	0.0133	1.0×10^{17}	3952	50	2.8
	Ratio #3/#1	1.0	14.3	17.2	22.6	21.4

The storage time ratios of Table 2.5 do not match the doping ratios exactly, but they fall within a factor of two difference. The experimental agreement is reasonable when one considers the processing differences that could account for changes in G_B and G_P. The films were grown in different MBE systems (Perkin-Elmer Model 400 versus a Varian Gen-II), and different chemical etchants (1 H_2SO_4 : 8 H_2O_2 : 40 H_2O versus 3 H_3PO_4 : 1 H_2O_2 : 25 H_2O) were used to define mesa perimeters.

Once the doping is high enough that field enhanced generation is significant, the experimental evaluation of capacitor storage time as a function of doping profile is a very tricky proposition. Due to the temperature and scaling dependences, direct comparisons of storage time carry quantitative meaning only when devices of like P/A ratios are considered at specific temperatures. Figures 2.33 and 2.34 are given as examples. The $P^+N^+P^+$ device of Figure 2.33 has longer storage times at high temperatures, but the lighter-doped $P^-N^+P^-$ device prevails at room temperature because it has a higher activation energy. The large and small $P^+iN^+iP^+$ devices of Figure 2.34 demonstrate that identical doping profiles can yield unlike storage time characteristics when the P/A ratio is different. Perimeter generation is more dominant in smaller devices, so τ_S is shorter in the smaller $P^+iN^+iP^+$ device. Furthermore since perimeter generation is less susceptible to high-field enhancement, the smaller device has a higher activation energy than its larger counterpart.

Despite the quantitative comparison difficulties mentioned above, it is useful to have some idea of built-in field at which bulk field-enhanced generation kills the storage time advantage predicted for increased doping. Even though it compares devices of unlike P/A ratio, the plot of τ_S versus T for the best devices recorded on each wafer gives a rough estimate (Figure 2.35). Field enhanced generation is substantially visible only for the $P^+N^+P^+$ device, whose built-in field is over 600 kV/cm (Table 2.4). It should be noted however that performance is seriously hampered only at T's approaching room temperature.

A worst-case analysis of the capacitors of Figure 2.35 reveals that all have sufficiently long storage times for use in room-temperature DRAM's. One can conservatively divide the storage times of Figure 2.35 by 100 to account for shrinking of device sizes from the largest experimental cell (300 x 300 μm^2, P/A = 0.0133 μm^{-1}) to a practical DRAM cell size (4 x 4 μm^2, P/A = 1.0 μm^{-1}). Under this assumption, all the capacitors meet the operational requirement (Section 2.0.1) of $\tau_S > 100$ mS for temperatures up to 60 °C.

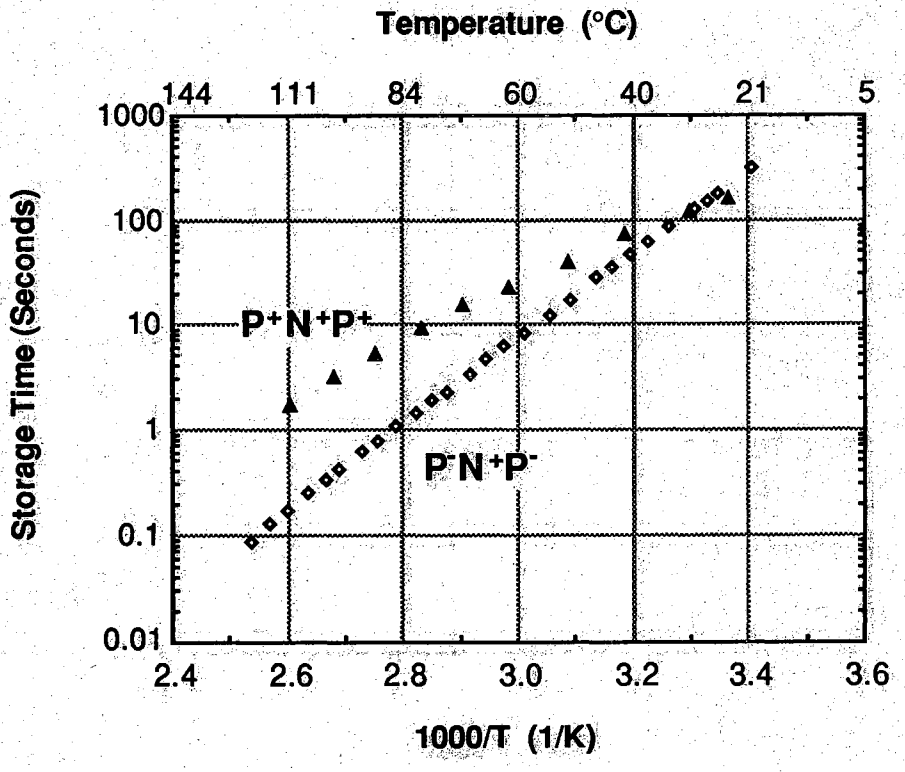


Figure 2.33 Storage time versus temperature comparison of capacitors with different activation energies.

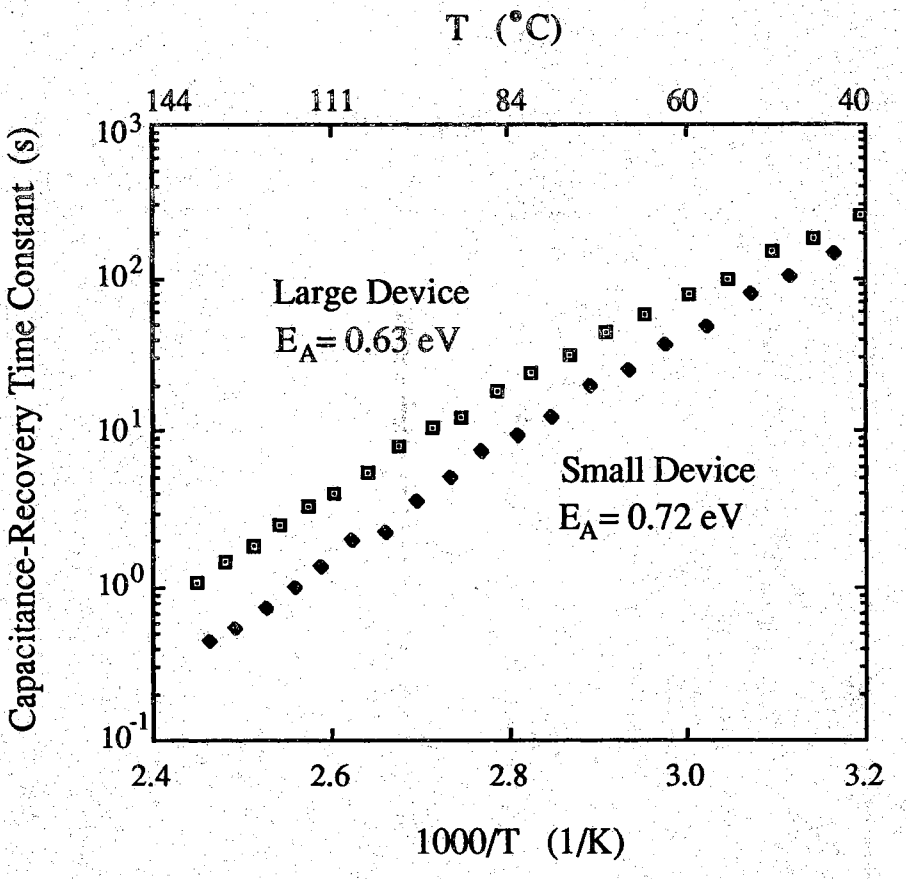


Figure 2.34 Storage time versus temperature comparison of large and small $P^+iN^+iP^+$ devices. The capacitors were fabricated on the same wafer, but the differences in P/A and the thermal behavior of G_B and G_P result in differing activation energies. After Reference [1].

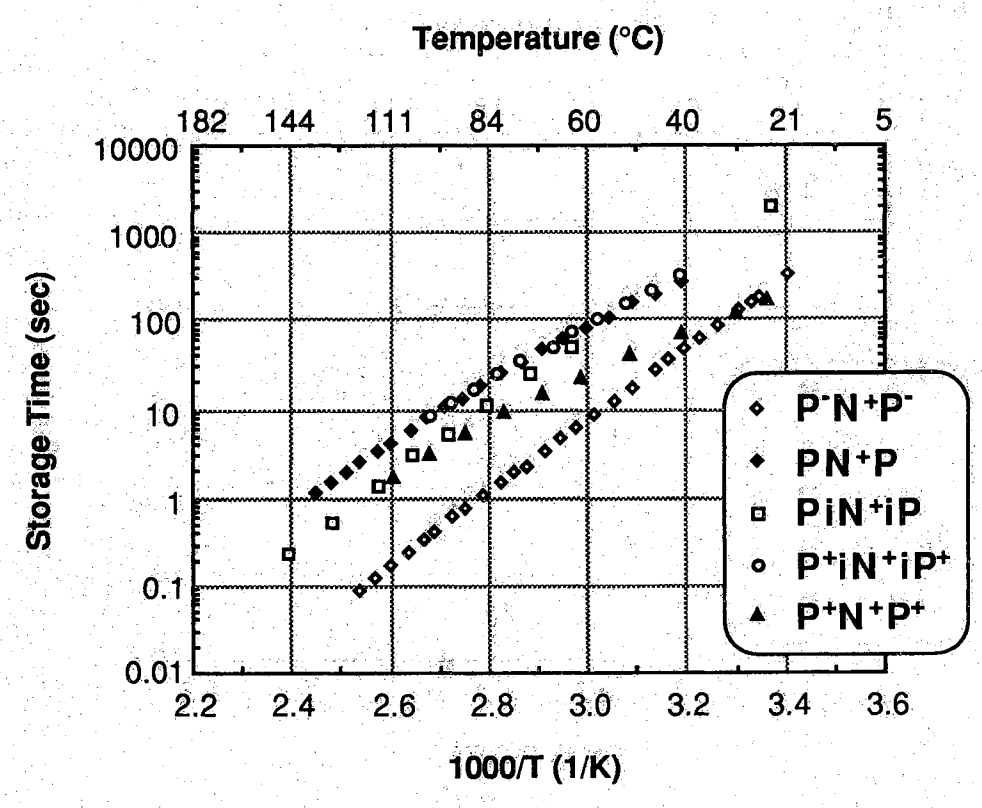


Figure 2.35 Comparison of large-area device storage times from various wafer doping profiles. Parameters for each wafer are given in Table 2.4.

Perhaps overlooked in the lengthy experimental discussion of storage time physics is the critical design capacitor goal of charge storage density. Given the achievement of sufficient room-temperature storage times for all doping profiles tested, the optimum capacitor is one that realizes maximum charge density. It would thus appear on the surface that the $P^+N^+P^+$ device with its high charge storage density (Figure 2.4) is the optimal choice for near room-temperature operation. If the DRAM needed to operate at significantly higher temperatures, one might switch to the $P^+iN^+iP^+$ device to increase storage time.

2.8 AlGaAs PiNiP Capacitors

The generation rates in Section 2.2 are proportional to n_i, which in turn is exponentially dependent on the bandgap. It therefore stands to reason that significant storage time gains might be achieved by implementing PNP capacitors in a wider-bandgap semiconductor, provided that changes in the bulk generation lifetimes (τ_{pB} and τ_{nB}) and surface recombination velocity s_o do not offset the reduction in n_i. The $Al_xGa_{1-x}As$ capacitor experiments described in this section attempted to document this effect. Results of the first experimental comparison of PNP structures fabricated in GaAs and $Al_{0.2}Ga_{0.8}As$ are shown in Figure 2.36, and as expected the $Al_{0.2}Ga_{0.8}As$ capacitors showed substantially larger storage times than their narrower-bandgap GaAs counterparts [1,11]. The extrapolated zero-temperature bandgap of $Al_{0.2}Ga_{0.8}As$ as calculated from parameters given in Reference 123 is 1.88 eV, so both samples exhibited near-half-bandgap activation consistent with the change in n_i. However, the actual gain in experimental storage time does not directly correspond to the reduction of n_i, so it follows that changes in the generation parameters (τ_{pB}, τ_{nB}, and s_o) between GaAs and $Al_{0.2}Ga_{0.8}As$ partially offset the improvement in n_i.

A detailed study of the physical generation mechanisms of $Al_{0.4}Ga_{0.6}As$ P^+iNiP^+ storage capacitors (Figure 2.37) was carried out in a more recent experiment [7]. The aluminum mole fraction of 0.4 was

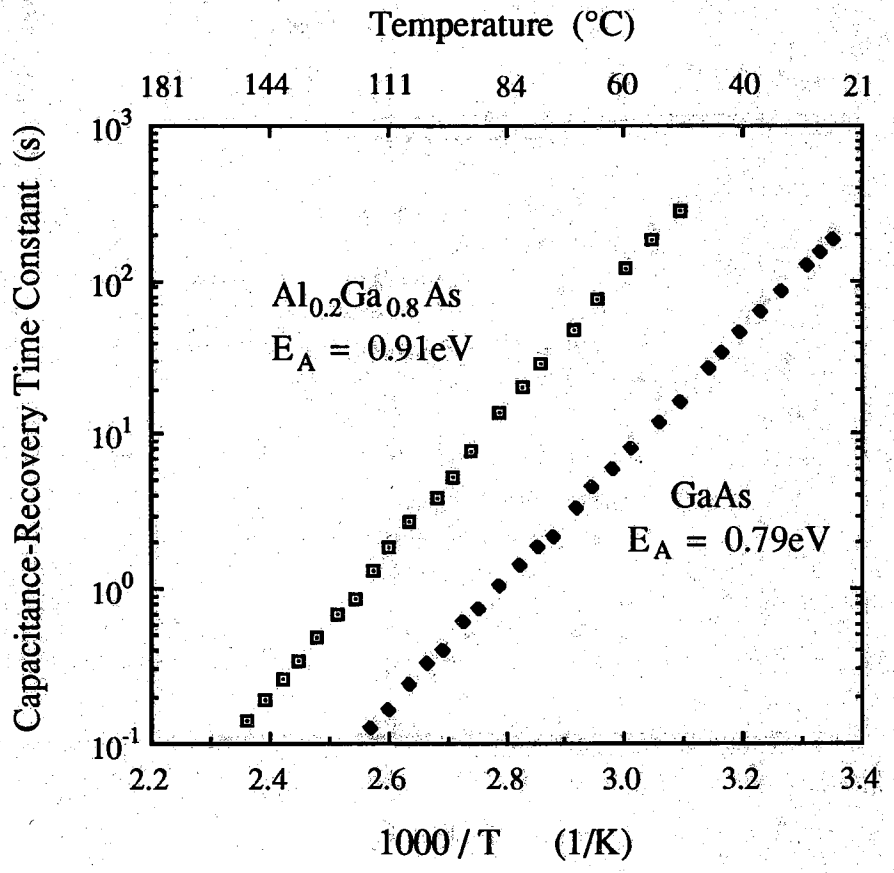


Figure 2.36 Storage time performance of comparable $Al_{0.2}Ga_{0.8}As$ and GaAs $P^-N^+P^-$ capacitors. Both devices had $N_A \cong 10^{16}$ cm^{-3} and $N_D \cong 10^{18}$ cm^{-3}. After Reference [1].

chosen to maintain a direct semiconductor band structure while minimizing n_i [123]. Figure 2.38 shows the storage time performance of four device sizes over the temperature range of 70 to 145 °C. The activation energies change with device size, and they do not correspond to half the extrapolated zero-temperature bandgap of $Al_{0.4}Ga_{0.6}As$ (Extrapolated $E_G/2$ = 1.11 eV as calculated from parameters in Reference [123]). The above half-bandgap activation suggests that generation at non-midgap centers is significant, and the trend of higher activation energies for smaller devices implies that the perimeter generation rate G_P has a higher activation energy than the bulk generation rate G_B.

To resolve the two mechanisms, the bulk and perimeter generation rates at each temperature were calculated by applying (2.34) to plots of $1/\tau_S$ versus P/A (Figure 2.39) as outlined in Section 2.3.2. The temperature dependence of the two mechanisms is presented in Figure 2.40. The bulk generation rate G_B exhibits near half-bandgap activation (E_A = 1.16 eV), and is consistent with the hypothesis that near-midgap surface states dominate thermal generation in the bulk. In contrast, the measured temperature dependence of G_P (E_A = 1.59 eV) does not conform with the supposition that near-midgap surface states dominate perimeter edge generation. Instead, the experimental behavior of G_P can be modeled within the framework of (2.22) by dominant surface generation centers that are approximately 0.5 eV off the middle of the bandgap. Whether these centers lie above or below E_i cannot directly be inferred from these measurements, due to the energetic symmetry of (2.22).

2.8.1 AlGaAs Storage Time Extrapolation

Prediction of low-temperature storage times from high temperature data is at best precarious. First of all, small errors in the measured activation energy can exponentially propagate themselves into misleading storage time predictions. Secondly, all sources of leakage must be properly taken into account. A careless prediction for the 100 x 100 μm $Al_{0.4}Ga_{0.6}As$ PiNiP device of Figure 2.38 involves simple extension of the

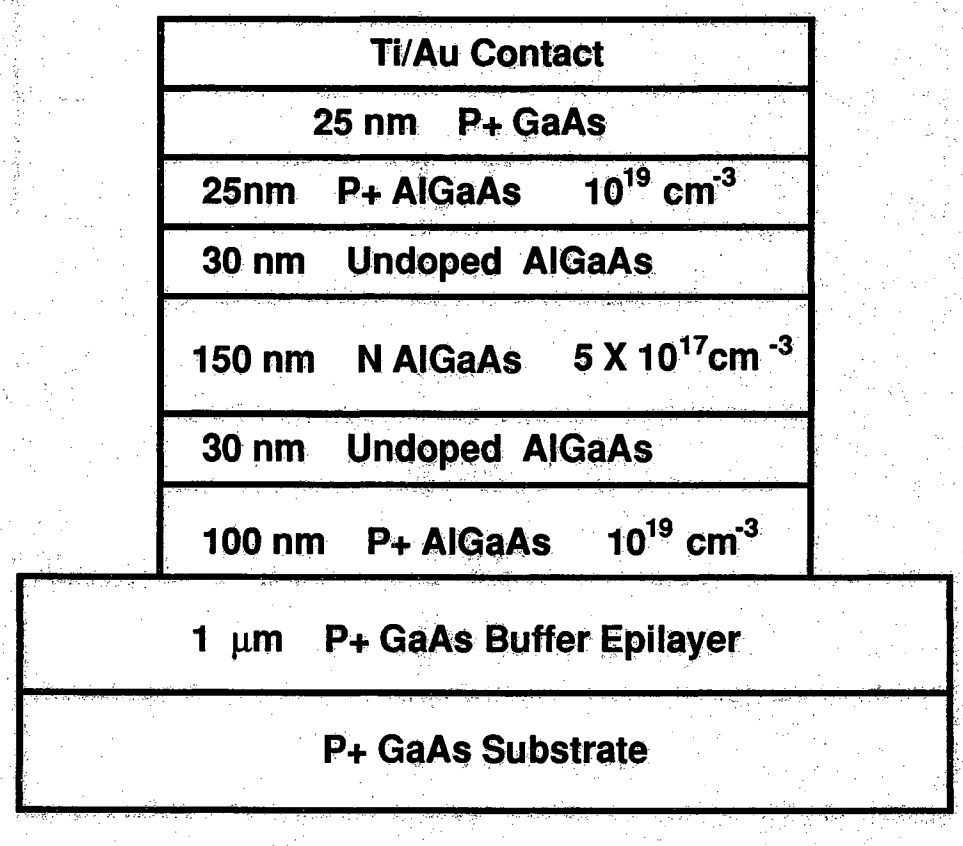


Figure 2.37 P^+iNiP^+ $Al_{0.4}Ga_{0.6}As$ capacitor cross-section. After Reference [7].

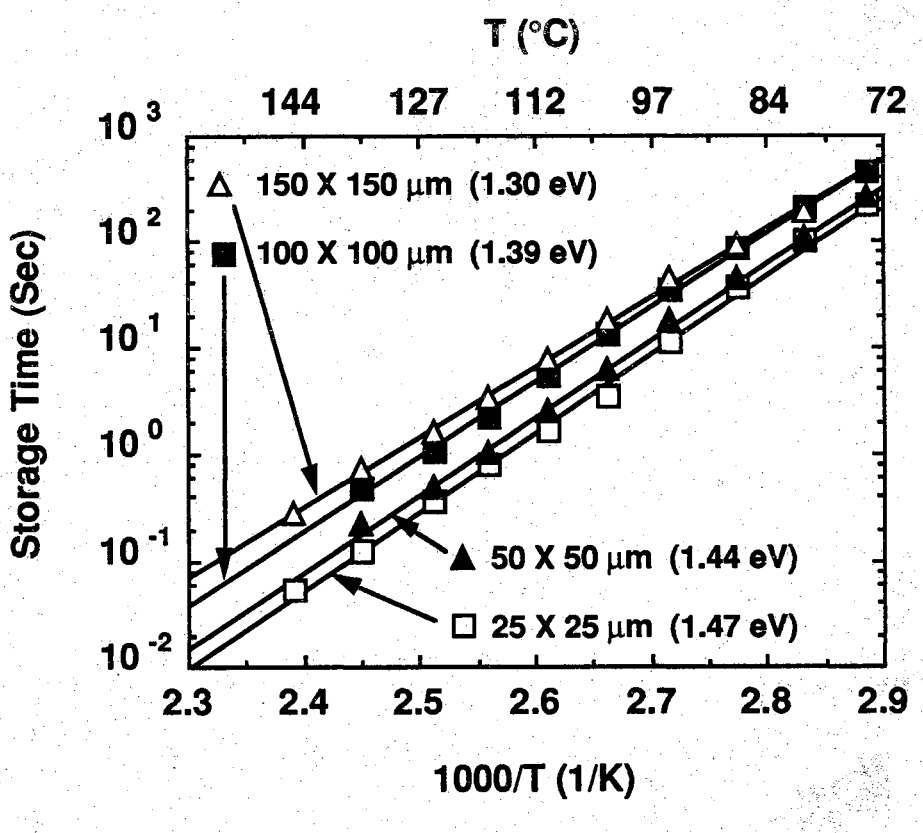


Figure 2.38 Storage time versus temperature data for $Al_{0.4}Ga_{0.6}As$ P^+iNiP^+ capacitors. The storage time and the activation energy changes with device size. After Reference [7].

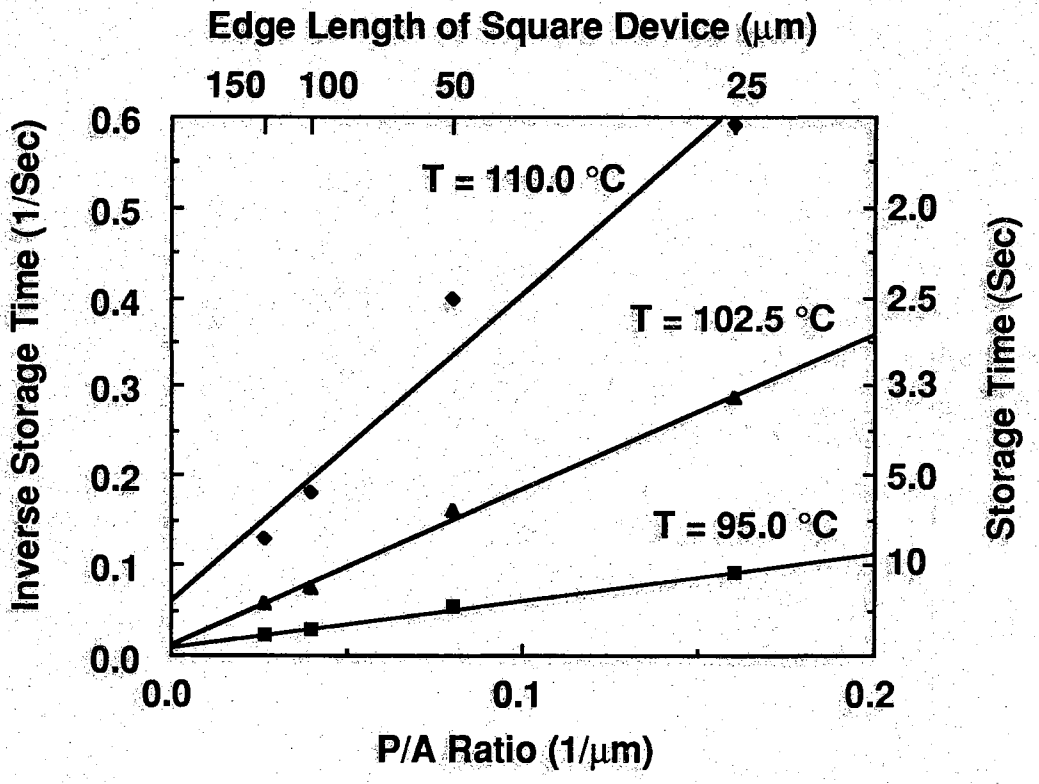


Figure 2.39 $Al_{0.4}Ga_{0.6}As$ capacitor inverse storage time as a function of P/A ratio for three different temperatures. The y-intercepts are proportional to the bulk generation rate G_B and the slopes are proportional to the perimeter generation rate G_P. After Reference [7].

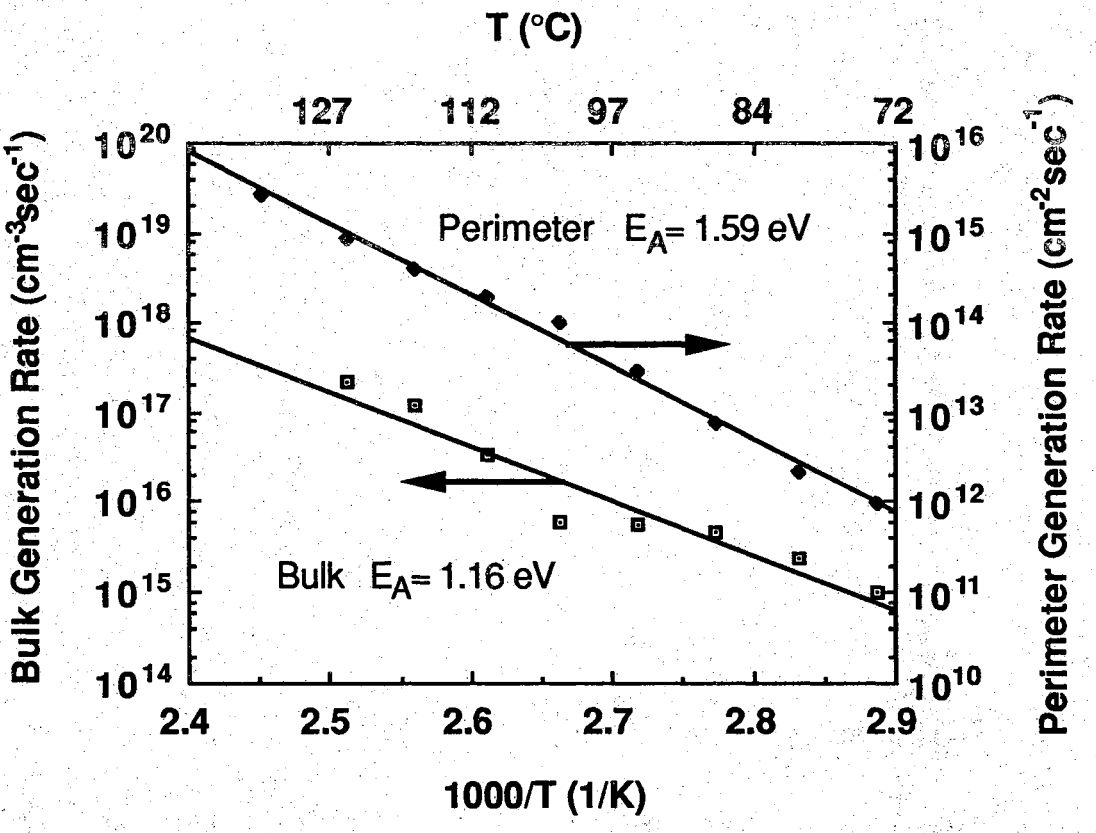


Figure 2.40 $Al_{0.4}Ga_{0.6}As$ bulk and perimeter generation rates as a function of temperature. After Reference [7].

E_A = 1.39 eV best fit line to room temperature, which yields an extrapolated τ_S of 166 hours. This simplistic approach ignores the fact that two separate mechanisms with differing activation energies are involved. Perimeter generation with its higher activation energy dominates at higher temperatures, while the low activation energy of the bulk generation component makes it become important at low temperatures. This is evidenced in Figure 2.38 by the run-together of the storage time data as the temperature drops. A more proper extrapolation of the storage time to room temperature is based on the lower bulk activation energy of 1.16 eV. This extrapolation yields a room temperature storage time of 50 hours.

The existence of a third leakage mechanism could easily invalidate this extrapolation. To throw off the prediction, this mechanism would have to have the lowest activation energy so that it would only become significant at lower temperatures than were measured experimentally. The possible existence of additional leakage mechanisms seriously casts doubt on the validity of extrapolating storage times to low temperatures. Though excruciating, one can only prove the existence of multi-hour storage times through direct measurement.

Figure 2.41 shows a storage time transient taken from a 200 x 200 μm $Al_{0.4}Ga_{0.6}As$ PiNiP capacitor at room temperature. The 1/e storage time constant, which was calculated via computerized exponential curve-fitting, is over 8 hours. This number is significantly lower than the room temperature extrapolations mentioned above. Practical laboratory considerations prevented the measurement of other devices however, so it is unclear whether the low storage time is due to a physical leakage mechanism that manifests itself at low temperature. A point defect of some kind may govern the storage time, and this would represent a yield problem instead of a fundamental physical device limitation.

2.9 The Surface Exposure Effect

The PNP and PiNiP capacitor structures presented in this report so far have had the same basic structure in common. All junctions have been

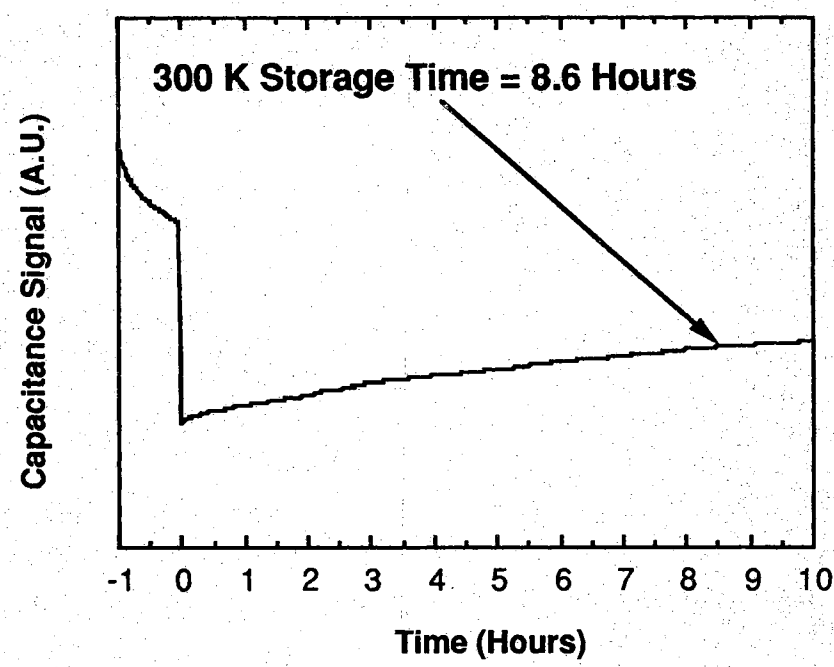


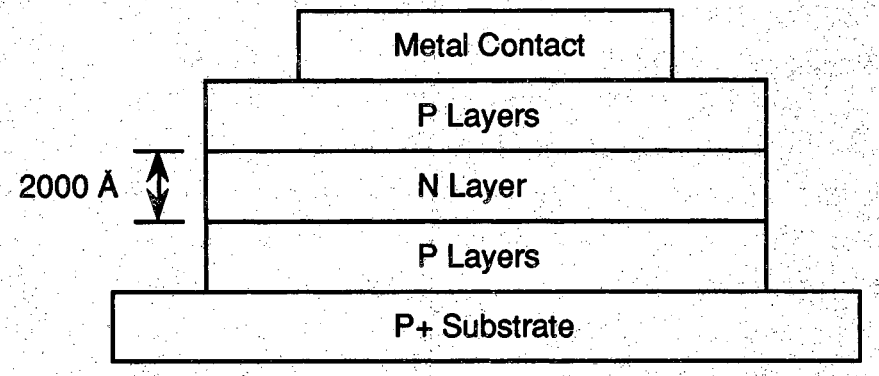
Figure 2.41 Room-temperature capacitance transient obtained from a 200 x 200 μm^2 $Al_{0.4}Ga_{0.6}As$ P^+iNiP^+ device. The light-off transient had not entirely decayed when the bias pulse was applied, so the 1/e storage time was calculated using exponential curve fitting.

in epitaxially-grown layers, and all devices are mesa-isolated by a single masking step as depicted in Figure 2.42a. However, the fabrication of a complete epitaxial GaAs DRAM cell (Chapter 4) requires that a horizontal surface of the sandwiched N-region be exposed, as depicted in Figure 2.42b. Alignment tolerances dictate that microns of N-GaAs be horizontally exposed (Figure 2.42b), whereas less than 2000Å of N material is typically surface-exposed in the simple vertical structure of Figure 2.42a. Given the high surface-state density of GaAs, the large increase in surface-exposed N-area could boost the surface generation current and decrease capacitor storage times.

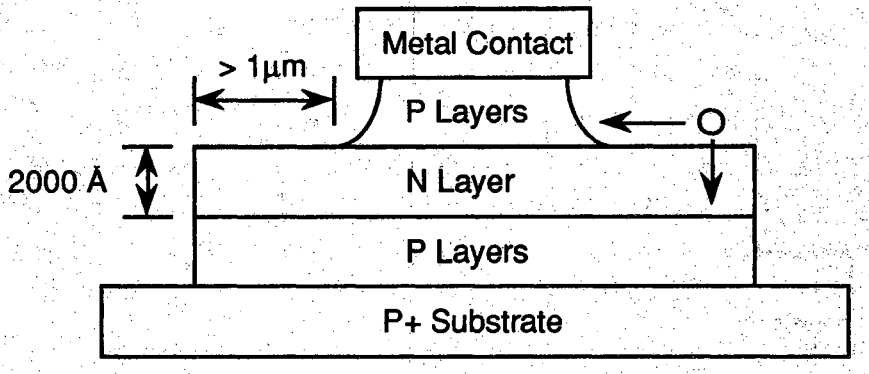
Theoretical arguments have been presented to dismiss the detrimental effects of large surface-exposed areas [11]. For an ehp thermally generated at the surface to discharge the storage node, holes must be removed to the P-region (Figure 2.42b). Outside the junction depletion region there is no electric field to carry in holes generated some distance away from the depletion region. Instead, generated holes must move to the junction by diffusion, either along the surface or through the bulk, if they are to affect the leakage performance of the device. However it was calculated in Reference [1] that bulk and surface diffusion currents were insignificant compared to surface generation current, so an increase in the surface-exposed area of the node should therefore have very little effect on capacitor storage time.

The experimental data collected so far strongly disputes the above arguments. Figure 2.43 compares the storage times of surface-exposed and non-surface-exposed devices from the same $Al_{0.4}Ga_{0.6}As$ PiNiP wafer (Figure 2.37). In addition to substantially reduced storage times, it worth noting that the surface-exposed samples exhibit no detectable perimeter-to-area variation, and apparent activation energies are also lower.

A similar investigation of GaAs devices is currently being undertaken, but results directly comparing surface-exposed and non-surface-exposed capacitors on the same wafer are not yet available. Nevertheless, Figure 2.44 shows strong evidence that leakage from surface exposure is substantial in GaAs. The data was taken from two GaAs P^+iNiP^+ capacitor films (same junction profiles as the $Al_{0.4}Ga_{0.6}As$ film of Figure 2.37) that match except for a difference in N-layer thickness. One



a) Conventional (non-surface-exposed) structure.



b) Surface-exposed structure.

Figure 2.42 Conventional and surface-exposed PNP capacitors. For generated holes to discharge the storage node, they must reach one of the junctions through either bulk or surface diffusion.

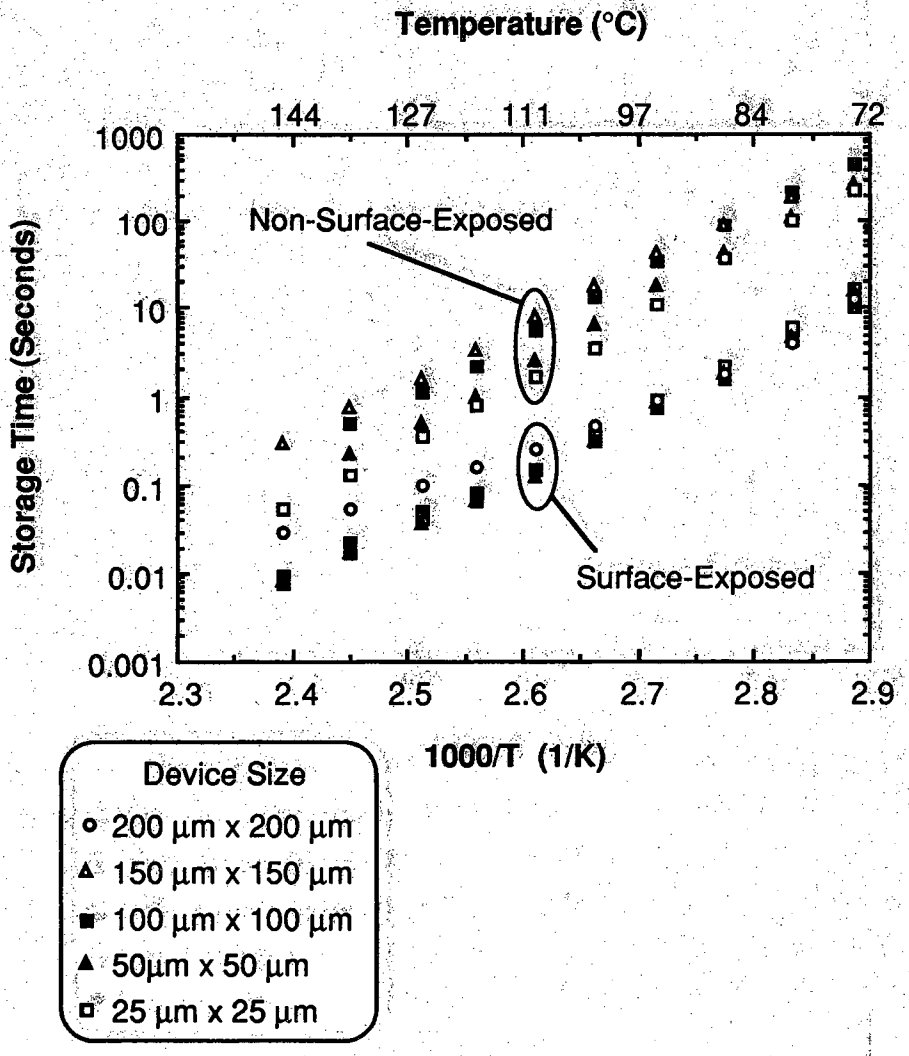


Figure 2.43 Experimental reduction in storage time of $Al_{0.4}Ga_{0.6}As$ P^+iNiP^+ samples from N-layer surface exposure.

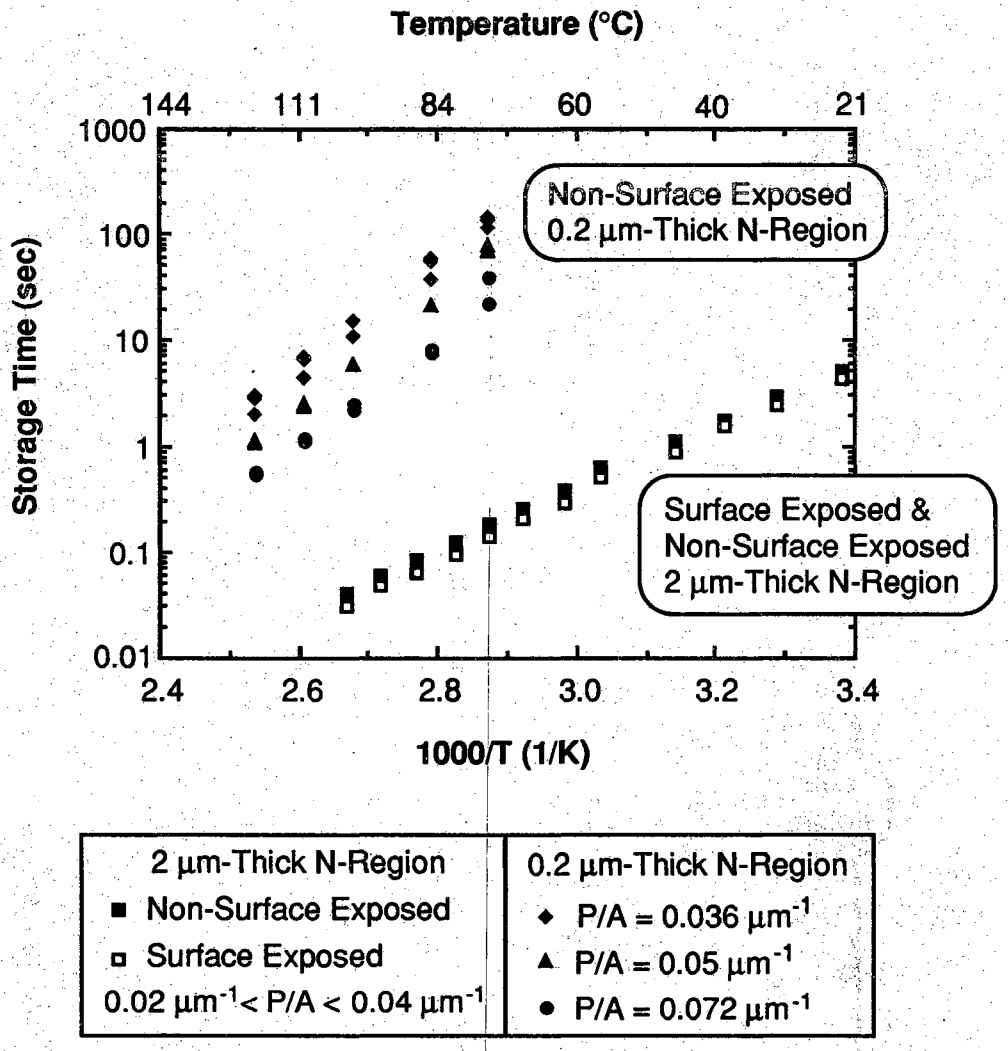


Figure 2.44 Storage time reduction caused by increasing the sandwiched N-region thickness from 0.2 µm to 2 µm. The 0.2 µm non-surface exposed devices show longer storage times and a clear P/A dependence, while the 2 µm thick N-region samples showed almost no detectable P/A variation.

film had a sandwiched N-layer thickness of 2000 Å while the other was 2 μm thick exposing a much larger surface area along the vertical sidewall. The measurements of Figure 2.44 show a huge difference in storage times between the two samples, and the activation energy has also been decreased. There is no detectable P/A variation in the 2-μm sample, whereas the 0.2-μm sample exhibits clear scaling with device size. Finally, some devices that were surface-exposed on the 2-μm sample (open squares in Figure 2.45) showed a very slight (< 20%) reduction in storage time over non-surface-exposed devices.

A detailed investigation into the scaling behavior of the surface-exposure phenomenon is currently in progress, and the results could shed light on the physical nature of the problem. The effect is severe enough that it could conceivably limit GaAs DRAM cell storage times.

2.10 Arsenic Sulfide Treatment to Reduce Surface Generation

As discussed in Section 2.3.2 and 2.7.3, storage times will decrease with shrinking capacitor size due to the increasing significance of perimeter generation. Recently however, there has been substantial progress in the use of chemical treatments to improve the electrical quality of the GaAs surface. Remarkable reductions in the surface recombination velocity s_o have been observed in GaAs solar cells and bipolar transistors whose surfaces have been treated with sulfide- and selenium-based solutions [15,19-22]. Because the surface recombination velocity s_o figures into the perimeter generation G_P rate via (2.23), these surface treatments show promise for reducing the unfavorable scaling dependence of PN junction storage capacitors, whereby τ_S decreases with shrinking device size.

The perimeter generation dominated ALE-grown PiN^+iP storage capacitors of Figure 2.27b were selected to undergo an As_2S_3 glass developed by E. Yablonovich et al. [21]. The treatment consisted of an oxide removal etch in 1 NH_4OH: 10 H_2O followed by a 5 minute soak in ammonium sulfide [16]. The sample was then rinsed in de-ionized water and placed in a solution of 0.16 M As_2S_3 dissolved in a 1 NH_4OH : 1

CH_3OH solution. After a spin-dry under flowing nitrogen, the sample was annealed at 280 °C under flowing N_2 for two minutes. This procedure leaves behind a robust As_2S_3 glass which passivates the etched capacitor sidewalls [21,22].

The results of storage time measurements taken before and after treatment are given in Figure 2.45. Regrettably, low ALE device yields prevented the accumulation of more than the three device sizes shown. Nevertheless, the data points taken prior to treatment (open symbols) show a clear perimeter-to-area storage time variation. Following treatment (filled-in symbols) the devices exhibited increased storage times, and the dependence of τ_S on device size is no longer discernable. This suggests that the perimeter generation current in the treated devices, which prior to treatment was the dominant leakage mechanism, has been reduced to the point where it is smaller than the bulk generation current for the size devices tested. The treated 100 x 100 μm device storage time is almost an order of magnitude greater than its untreated counterpart.

2.11 Trenched Diodes Grown By Atomic Layer Epitaxy

Many silicon DRAM cells employ trenched storage capacitor technologies (Figures 2.1 and 2.2) to increase charge storage densities [59,60], so it is appropriate that this research investigated trenched PN junctions for use as GaAs storage capacitors. Fabrication of trenched analogs to the epitaxial storage capacitors presented in this work would on the surface appear unlikely, as uniform high-quality GaAs would have to be grown on trench sidewalls and corners. Previous efforts to grow GaAs 3-D structures using metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) have to date proven inadequate due to epilayer nonuniformities [101-104].

Atomic layer epitaxy (ALE) is a growth technique that proceeds in a self-limiting fashion so that growth takes place on all crystal surfaces with greater uniformity [105]. ALE has demonstrated a unique sidewall growth capability which could be exploited to produce epitaxial trenched PN

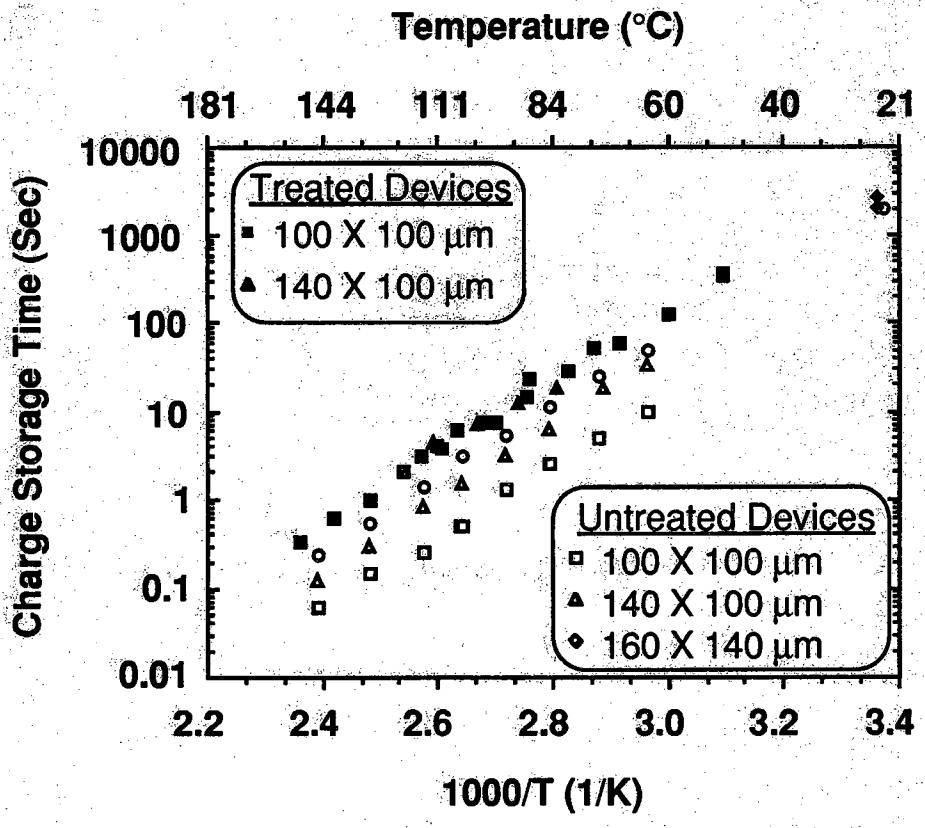


Figure 2.45 Increased storage times brought about by reduction of perimeter edge generation through As_2S_3 surface passivation.

junction storage capacitors [106-108]. However, previous work regarding sidewall ALE has failed to address the electrical quality of the sidewall material. Therefore to characterize the electrical quality of ALE-grown sidewall material and to investigate this possibiltiy of trenched epitaxial PN junction storage capacitors, a study of PiN diodes grown by ALE in trenches and sidewalls was undertaken [5,6].

PiN diode structures analagous to Figure 2.46 were fabricated using the procedure outlined in Reference [6]. The measured depth of the trenches was 2 μm, and the exact junction profiles are the same as those in Figure 2.27a. It should be noted that proper preparation of the substrate prior to growth is critical, as it seriously affects the quality of the subsequently-grown ALE material.

Leakage currents due to the trenches were characterized using the three 100 x 100 μm diode structures. One diode has a planar top surface, one contains a single 30 x 30 x 2 μm trench (Figure 2.46), and one contains nine 10 x 10 x 2 μm trenches. The total horizontal surface area is the same (10^4 μm^2) on each of the three diode mesas. Moreover, the horizontal area at the bottom of trenches is exactly 900 μm^2 on both the 1-trench and the 9-trench samples. The only difference between the 1-trench and 9-trench samples is the trench perimeter (which has a 3:1 ratio) and the number of trench corners (which has a 9:1 ratio). An independent test structure was used to verify that material in the bottom of the trenches is electrically connected to the top planar surfaces via the ALE-grown sidewalls.

At room temperature the reverse diode leakage currents were below the noise limit of conventional current measurement equipment, so I-V characterization was conducted at 144 °C. The I-V curves of the three 100 x 100 μm diodes are given in Figure 2.47 along with the I-V curve of a 100 x 100 μm low-leakage diode (the PiN^+ diode of Figure 2.27a in Section 2.7.3) which was fabricated on a planar substrate with no trenches. The nearly identical characteristics of the two planar diodes shows that planar material on the trenched substrate is comparable to the excellent material reported in Reference [4] and Section 2.7.3. Planar devices fabricated entirely on the flat bottom surfaces of large trenches show the same leakage characteristics as planar devices on the top surface.

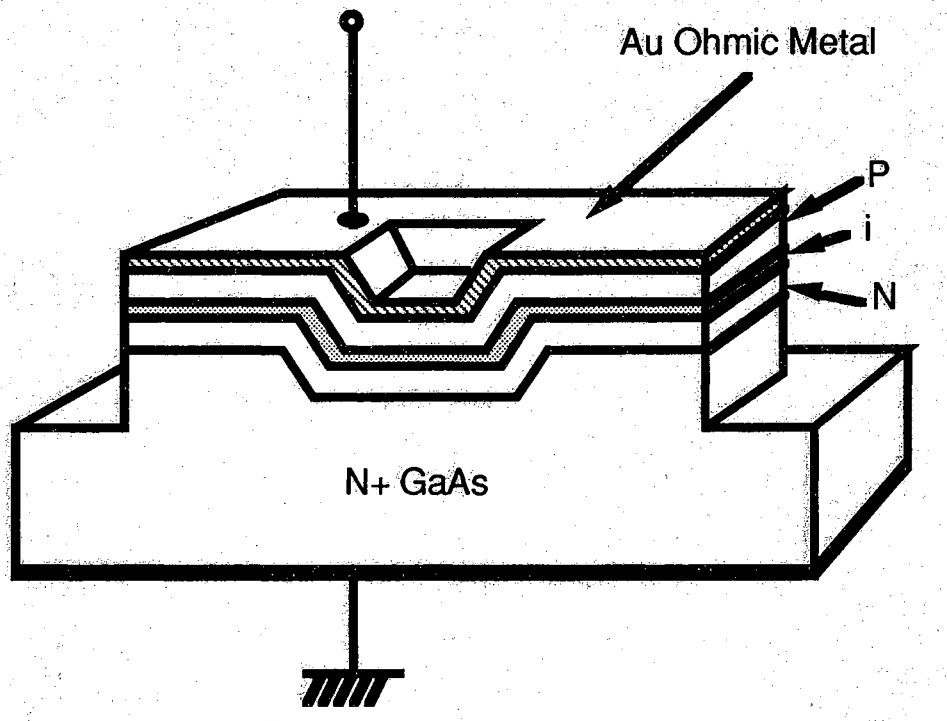


Figure 2.46 Schematic cross-section of a single-trench mesa-isolated PiN diode. The PiN^+ junction profile for this device is the same as the one given in Figure 2.27 of Section 2.7.3. After Reference [4].

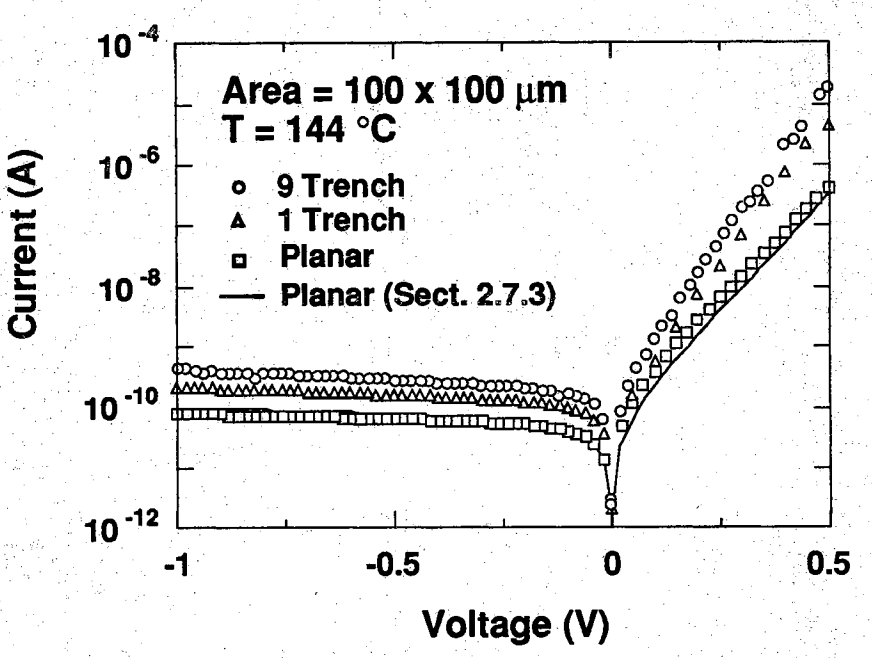


Figure 2.47 High temperature ALE PiN$^+$ diode I-V characteristics. The reverse current increases roughly as the square root of the voltage, indicating that thermal generation remains the dominant leakage mechanism. After Reference [4].

Figure 2.48 shows the dependence of leakage on trench perimeter for several devices of each type. A general linear dependence is apparent, indicating that sidewall leakage scales directly with trench perimeter and not with the number of trench corners. It is not possible from this data to determine whether sidewall leakage actually scales with sidewall perimeter or with sidewall area, since all trenches are the same depth. Further experiments are planned to determine the dependence on trench depth and on trench orientation. However, if the sidewall leakage component is normalized to sidewall area for these samples, we obtain a value of about 60 $\mu A/cm^2$ at 144 °C and 1 V reverse bias which is quite satisfactory for many device applications. However, this number is 60 to 100 times larger than the values reported for comparable planar ALE diodes in Table 2.1.

The reverse-bias sidewall current varies approximately as the square root of applied voltage, which suggests that thermal generation in the depletion region is the primary source of sidewall leakage. The temperature dependence of leakage current at 1 V reverse bias for the three 100 x 100 μm diodes is given in Figure 2.49. The activation energy of leakage current on the 1-trench and 9-trench diodes are nearly the same, at 0.844 eV, while the activation energy of the planar sample is 0.713 eV.

2.12 PN Junction Capacitors on Lightly-Doped Substrates

The symmetric PNP and PiNiP capacitor structures provide an excellent basis for the study of diode charge storage physics. In real life however, most GaAs JFET and MESFET IC's are manufactured on insulating substrates. Though PNP-like capacitors can still be implemented within the framework of this technology, it is often simpler to use a P^+N capacitor on undoped insulating material (Figure 2.50). Though its behavior is similar to the PNP capacitors studied previously, there are some important differences that are noted in this section.

Undoped insulating GaAs is usually p-type in nature, so a P^-N diode is effectively formed at the bottom. The lighter-side doping of the bottom junction is much less than the top junction, so effectively the entire charge is stored by the top junction. As a result, the P^+NP^- structure of Figure

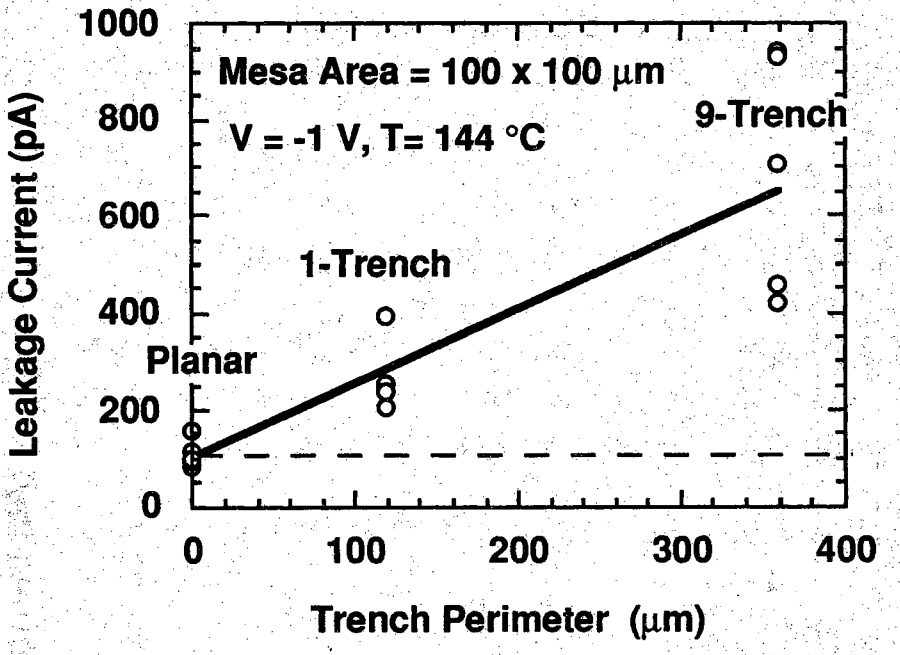


Figure 2.48 Trench ALE leakage current as a function of trench perimeter.

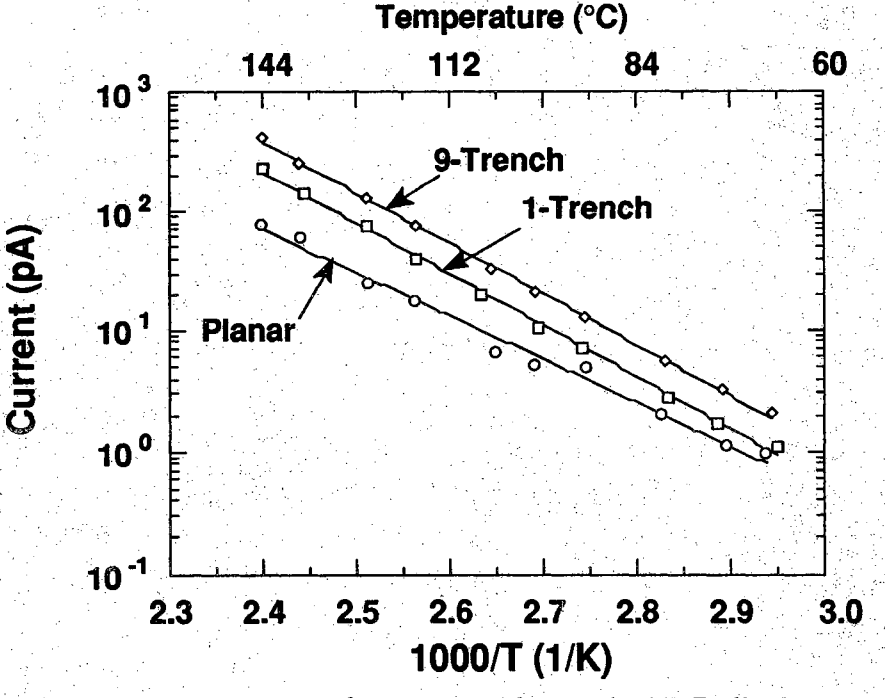


Figure 2.49 Temperature performance of trench ALE diodes.

2.50 has only half the charge density of a similarly-doped P^+NP^+ capacitor which holds equal charge on the top and bottom junctions. Most of the reverse leakage should be due to thermal generation of electron-hole pairs in the large depletion region associated with the bottom junction. If the generation width reaches as far down as the epilayer-substrate interface (Figure 2.50), the problem could be exacerbated by the numerous interfacial defects known to exist at this boundary [15,114]. Buffer epilayers should therefore be designed to prevent this condition from occurring.

The detrimental effects of the large lower junction depletion are bourn-out in the experimental storage time performance of P^+NP^- capacitors fabricated during FET processes (Table 2.6). These capacitors incorporate a 500 Å thick buried P layer (Figure 2.50), the purpose of which is to suppress epitaxial FET short channel effects (Chapter 3). The 500 Å P layer is entirely depleted by the heavier doped N-region at zero bias, but it has the positive effect of reducing the lower-junction depletion/generation depth. Although the storage times are well below those recorded on symmetric PNP structures (Figure 2.35), they still appear sufficiently long for use in a room temperature DRAM. As these capacitors were surface-exposed (Figure 2.50), some of the performance degradation may be due to the surface-exposure effect presented in Section 2.9.

Because their storage time is longer, the most notable devices of Table 2.6 come from the DCAM wafer. The DCAM storage capacitors were unique in two aspects. A thicker P^+ cap layer was employed (750 Å as opposed to the 500 Å shown in Figure 2.50), and most of their exposed-surfaces were polyimide-passivated. The scaling behavior of DCAM capacitors is shown in Figure 2.51. Since the bottom junction is expected to dominate the leakage characteristics, the P/A plot is referenced to the mesa size instead of top P^+N diode size. The best-fit line suggests that a 4 x 4 μm^2 capacitor will have a storage time of over a half-second at room temperature.

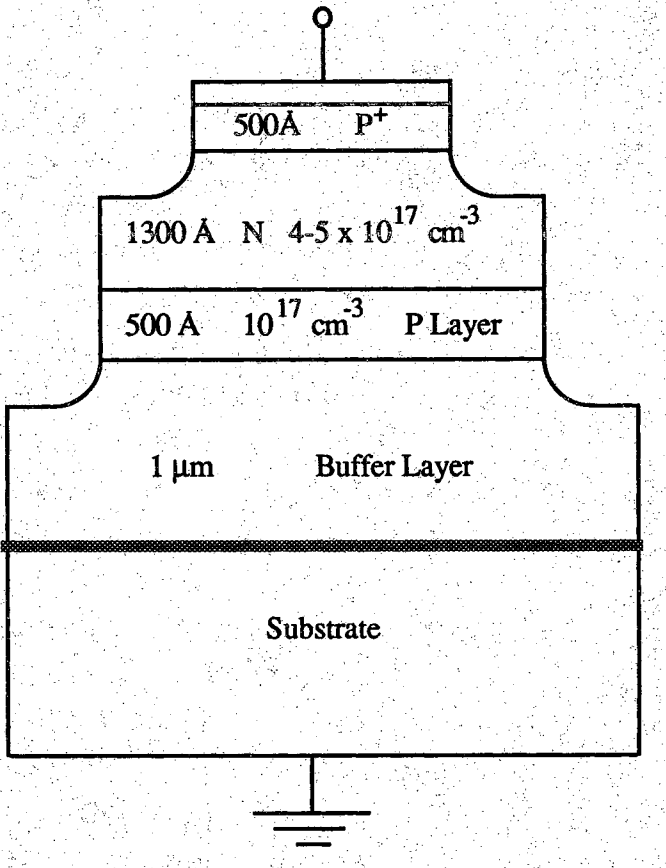


Figure 2.50 P^+NP^- capacitor cross-section. The devices are surface-exposed, and the buffer layer doping is varied slightly. The storage time of these devices should be governed by the lightly-doped lower junction.

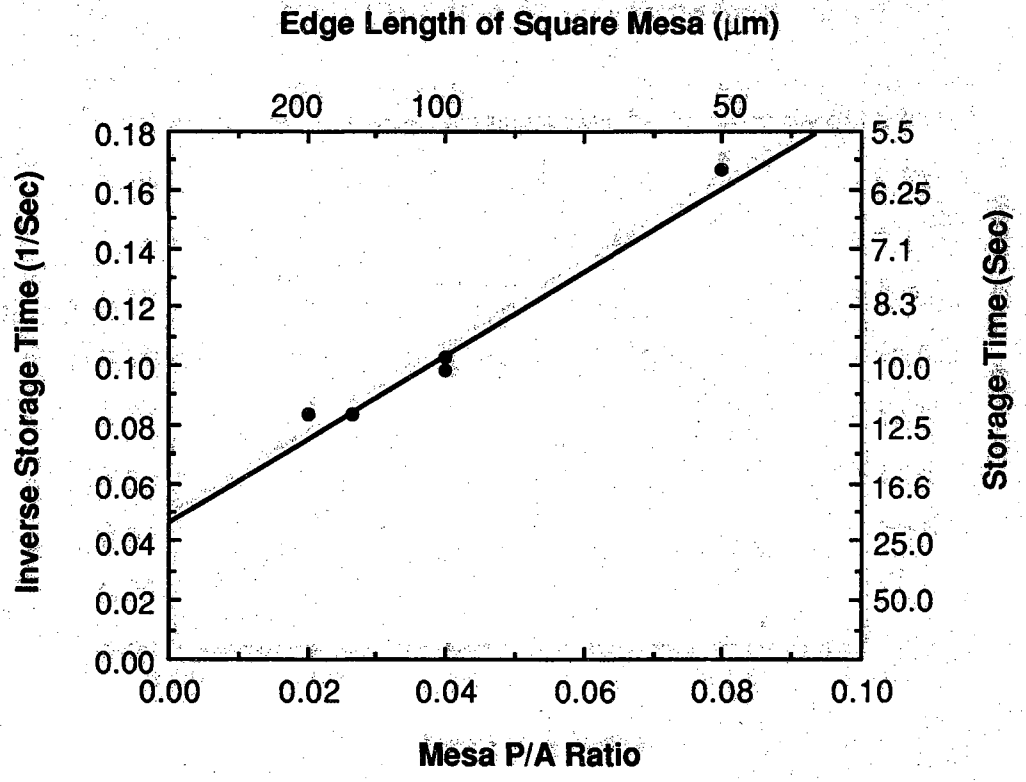


Figure 2.51 DCAM P^+NP^- capacitor storage time at 25 °C as a function of device size.

Table 2.6 Storage time performance of epitaxial FET-compatable P^+NP^- surface-exposed capacitors. The capacitor cross-section is given in Figure 2.50.

Sample	500 Å P Layer Doping (cm^{-3})	Buffer Layer P Doping (cm^{-3})	25 °C Storage Time (Seconds)	Activation Energy (eV)
P-Buffer JFET	5×10^{16}	5×10^{16}	4 - 5	-
I-Buffer JFET	10^{17}	$\sim 10^{15}$	3	0.60 eV
MESFET #1	10^{17}	$\sim 10^{15}$	1.5	-
MESFET #2	10^{17}	$\sim 10^{15}$	1.4 - 1.7	-
DCAM	10^{17}	$\sim 10^{15}$	6 - 12	-

2.13 Implanted Junction Storage Capacitors

One of the explicit research goals stated in Chapter 1 was the implementation of GaAs DRAM's in the JFET and MESFET technologies already in widespread use. Specifically these are planar ion-implanted FET technologies, so it is likely that a practical GaAs DRAM cell would have an implanted PN junction capacitor, as opposed to the epitaxially-grown junctions that have been studied in this chapter.

Experimental studies suggest that ion-implanted PN junctions are not much different from epitaxial PN junctions, both in terms of the low-leakage performance and the physical nature of the limiting mechanisms. Loh et. al. conducted an experimental study of diodes formed by Mg P^+ implants into lightly doped (2-3 x 10^{16} cm^{-3}) N-type layers, and thermal generation was documented to be the chief reverse-leakage mechanism [14]. The reverse current roughly increased as the square root of the voltage, and the reverse leakage exhibited half-bandgap thermal activation (E_A = 0.79 eV). As part of this work an experiment very similar to a PNP storage time measurement was carried out on an MIS-C/PN structure, and

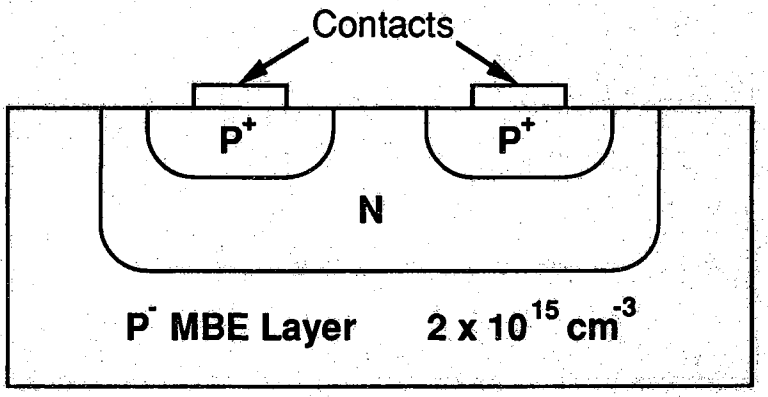


Figure 2.52 Ion-implanted P+NP- capacitor structure investigated by Pabst et. al. After References [12] and [13].

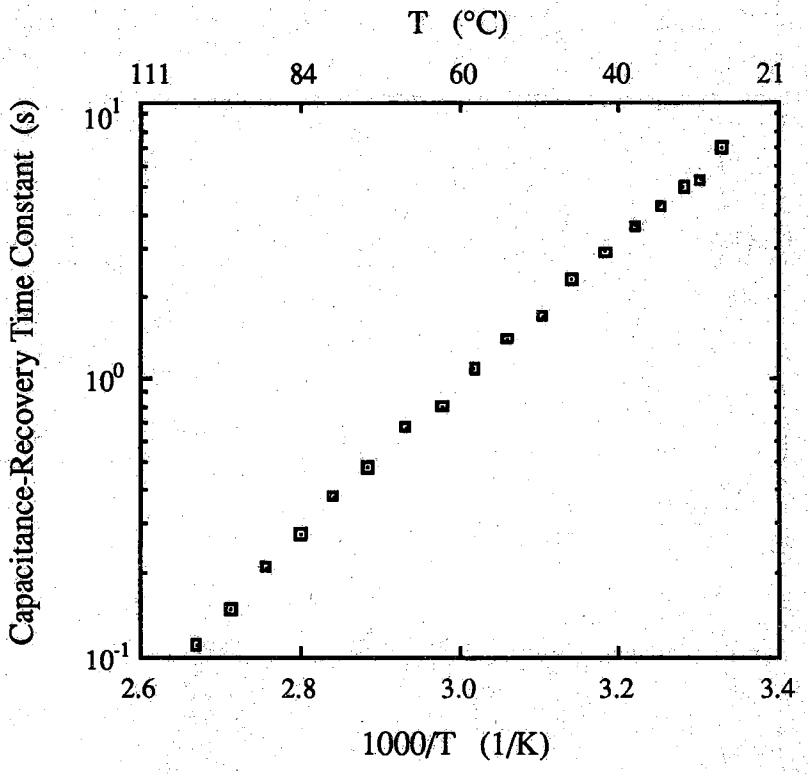


Figure 2.53 Storage time performance of ion-implanted P^+NP^- capacitor. $E_A = 0.516$ eV. After References [12] and [13].

it produced transients with time constants greater than 20 seconds at room temperature [14].

An experiment on actual PNP capacitors defined by ion-implantation was carried out by Pabst et. al. [12,13]. Both the top P region and the N-type storage node were defined by implantation, as shown in Figure 2.52. The storage time performance as a function of temperature is plotted in Figure 2.53, and it includes a τ_S of 8 seconds at room temperature. The results are quite comparable to the epitaxial capacitors of Table 2.6, especially when one considers the parallels in device structure. The lower junctions of both structures consist of lightly-doped p-material, and large areas of the N-type storage node are surface-exposed.

2.14 Schottky Diode Storage Capacitors

In the same manner that PN junctions can be used to store charge, metal-semiconductor Schottky diodes can also function as charge storage elements. Such a capacitor could be easily integrated into current high-yield LSI MESFET processes (as discussed in Section 4.4). Unfortunately, reverse leakage in Schottky diodes is very different from the thermal generation mechanisms that govern reverse leakages in PN junctions. Therefore a new storage capacitor theory that takes the different reverse-bias Schottky leakage physics into account must be developed.

2.14.1 Reverse-Bias Schottky Diode Leakage

An excellent description of Schottky barrier junction physics is given in References [23] and [24], but the major results that apply to this work are summarized here for completeness. Band diagrams for a GaAs Schottky barrier to N-type GaAs at equilibrium and reverse-bias are given in Figure 2.54. The depletion width W at applied bias V_A is given by [23]:

$$W = \sqrt{\frac{2\varepsilon_S}{qN_D}(V_{bi} - V_A)} \tag{2.77}$$

The built-in junction voltage V_{bi} is given by:

$$V_{bi} = (\phi_{bn} - \Delta\phi) + kT \ln\left(\frac{N_D}{N_C}\right) \tag{2.78}$$

where $\phi_{bn} - \Delta\phi$ is the effective junction barrier height at zero-bias (Figure 2.54a). For the one or two volt biases that would be encountered in a digital GaAs application, the chief reverse-bias leakage is thermionic emission of electrons over the junction potential barrier. The thermal generation of carriers in W does take place, but this mechanism is insignificant compared to carriers leaked by thermionic emission. The theoretical thermionic emission current density at applied forward voltage V_A is [24]:

$$J = J_S \exp\left(\frac{qV_A}{nkT}\right)\left[1 - \exp\left(\frac{-qV_A}{kT}\right)\right] \tag{2.79}$$

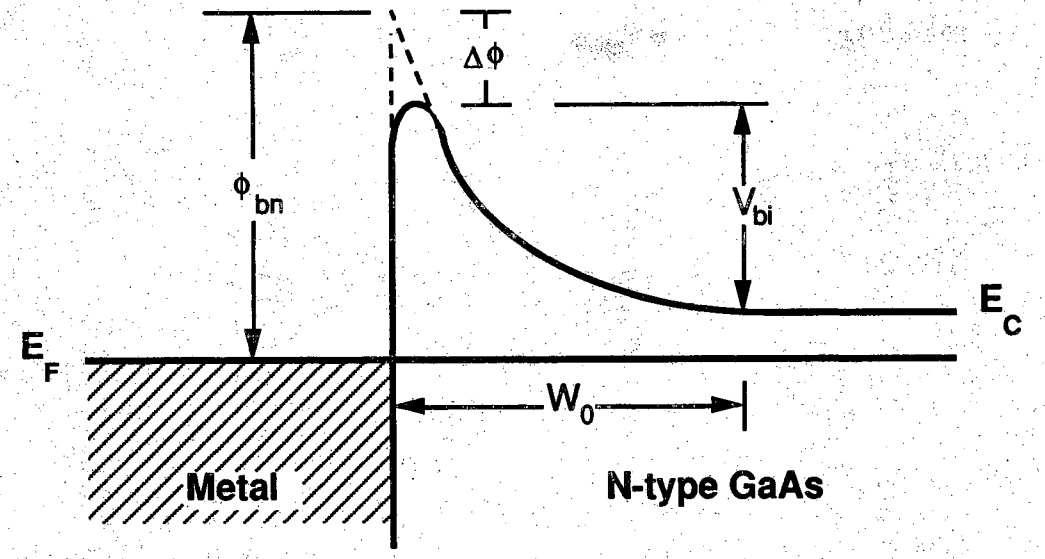
where J_S is the saturation current density and n is the ideality factor. The saturation current density J_S is given by:

$$J_S = A^*T^2 \exp\left[\frac{-q}{kT}(\phi_{bn} - \Delta\phi)\right] \tag{2.80}$$

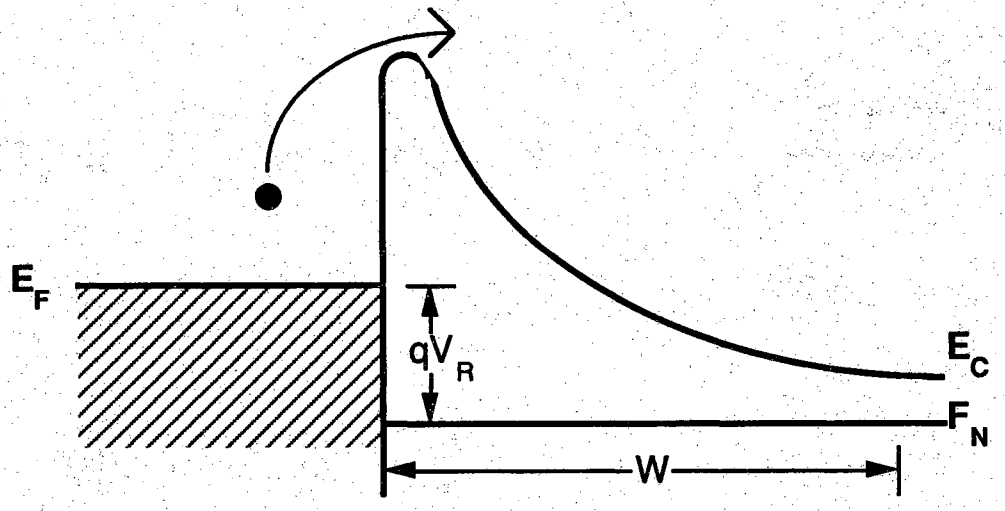
where A* is the effective Richardson constant. For any appreciable reverse bias V_R, (2.79) simplifies to a reverse bias current density J_R of:

$$J_R = J_S \exp\left[\frac{qV_R}{kT}\left(1 - \frac{1}{n}\right)\right] = A^*T^2 \exp\left[\frac{-q}{kT}(\phi_{bn} - \Delta\phi)\right] \exp\left[\frac{qV_R}{kT}\left(1 - \frac{1}{n}\right)\right] \tag{2.81}$$

The reverse Schottky diode leakage is exponentially dependent on the



a) Equilibrium



b) Reverse bias

Figure 2.54 Schottky barrier conduction band diagrams.

effective junction barrier height $\phi_{bn} - \Delta\phi$, the applied reverse voltage V_R, and the ideality factor n.

To make sense of the exponential dependences of (2.81), one must look at experimental results collected to date for Schottky barriers to N-type GaAs. In an ideal Schottky with no charged electrical defects at the metal-semiconductor interface, the barrier height would be determined by the metal-to-semiconductor workfunction difference [15,23]. Unfortunately the physical properties of the metal-GaAs interface are dominated by electrically active surface states. These surface states effectively pin the surface Fermi level near midgap, and result in a Schottky junction barrier height that is essentially independent of the metal-to-semiconductor workfunction [15]. As can be seen from (2.80), the GaAs barrier height invariance causes experimental saturation currents (J_S) to take on a limited range of values in spite of wide variations in fabrication techniques and materials.

Figure 2.55 shows a measured and theoretical J-V plot of an aluminum Schottky barrier to N-type ($N_D = 2.2 \times 10^{16}$ cm^{-3}) GaAs. Parameters for the theoretical plot were extracted from the measured forward biased characteristics (untreated Al entry of Table 2.7). The Schottky reverse leakage current densities are far above those measured in PN junctions (Section 2.7), which confirms the supposition that thermal generation in the Schottky diode space-charge region is insignificant compared to thermionic emission at the reverse biases of interest.

2.14.2 Schottky Storage Capacitors

When physically implemented on a GaAs wafer, Schottky storage capacitors could take the form of Figure 2.56, a Schottky-N-P (SNP) configuration. Because the N-layer is sandwiched by diodes with very different characteristics, these devices would most likely feature the asymmetric bias pulse behavior outlined in Reference [1]. As such it is possible that only one bias pulse polarity would charge the N-region to a positive potential. With the N-region charged to $+V_R$, the total charge on

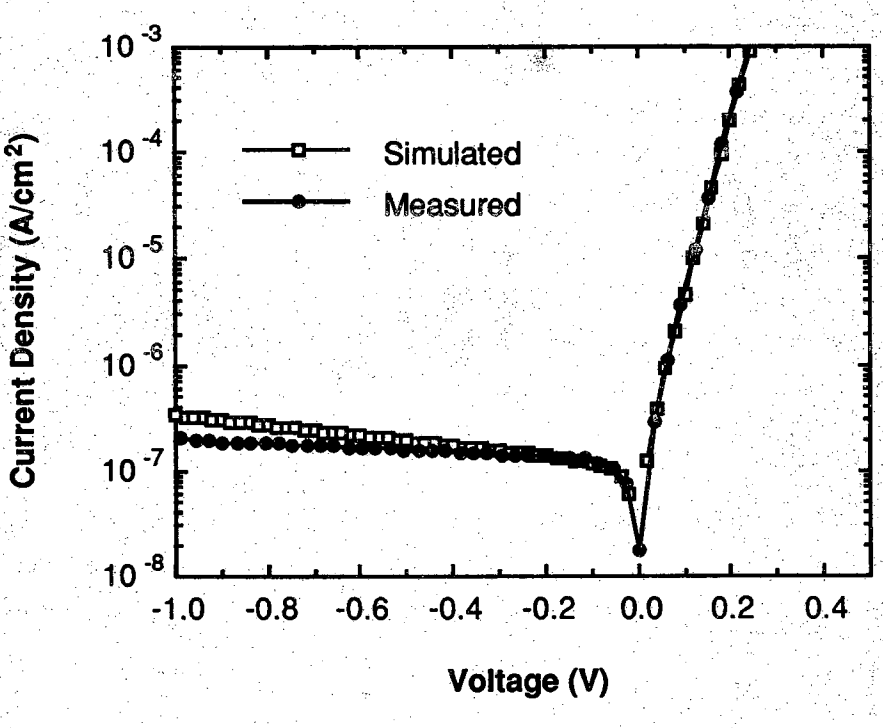


Figure 2.55 Measured versus theoretical J-V for an aluminum Schottky barrier. The theoretical reverse-bias current computed using parameters extracted from forward-biased measurements is larger than the actual measured reverse-bias current.

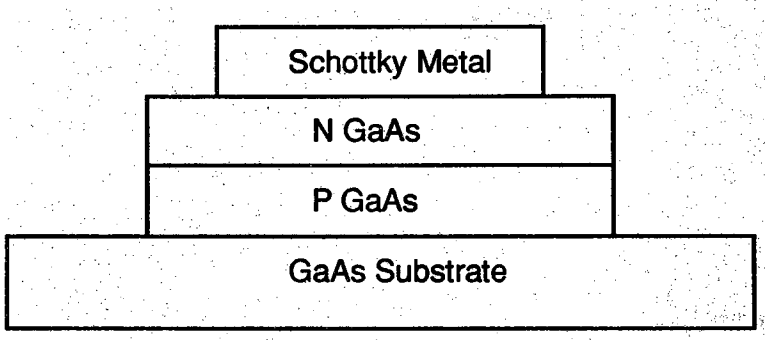


Figure 2.56 The Schottky-N-P (SNP) charge storage capacitor.

the capacitor is the total number of carriers missing from the enlarged depletion widths on top and bottom:

$$Q = Q_{PN} + Q_{SB} = qA\left[\left(\frac{N_D N_A}{N_D + N_A}\right)(W_{PN} - W_{PN0}) + N_D(W_{SB} - W_{SB0})\right] \tag{2.82}$$

where W_{PN} and W_{PN0} refer to PN junction depletion widths (2.2) and W_{SB} and W_{SB0} refer to Schottky barrier depletion widths (2.77), and A is the area of the device. If the P substrate doping is much less than the N-doping, or if a semi-insulating substrate is employed, (2.82) effectively reduces to:

$$Q = Q_{SB} = qAN_D(W_{SB} - W_{SB0}) \tag{2.83}$$

Aside from the difference in built-in junction potential, reverse-biased charge depletion of a Schottky barrier is nearly identical to the one-sided PN step junction [23]. It is therefore not surprising that the theoretical Schottky charge storage densities of Figures 2.57 and 2.58 are very similar in behavior to the PN junction charge storage densities of Figures 2.4 and 2.5.

Although the plot of Figure 2.57 includes doping densities greater than $10^{18}/cm^3$, the rectifying qualities of the Schottky barrier would come into question at degenerate dopings as significant tunnelling might occur [23,24]. A potential remedy to this problem might be the insertion of a thin undoped layer at the semiconductor surface to form a Schottky-i-N diode. The i-layer thickness would be governed by similar charge-density versus leakage-current design trade-offs discussed in Section 2.5 for the PiN junction, except that tunnelling replaces field enhanced generation as the primary source of undesired leakage.

Because the PN junction reverse leakage is much less than the leakage of the Schottky diode, the storage time of the SNP capacitor should be exclusively governed by the leakage of the top Schottky barrier. Thus the leakage of charge off the N-region will be governed by:

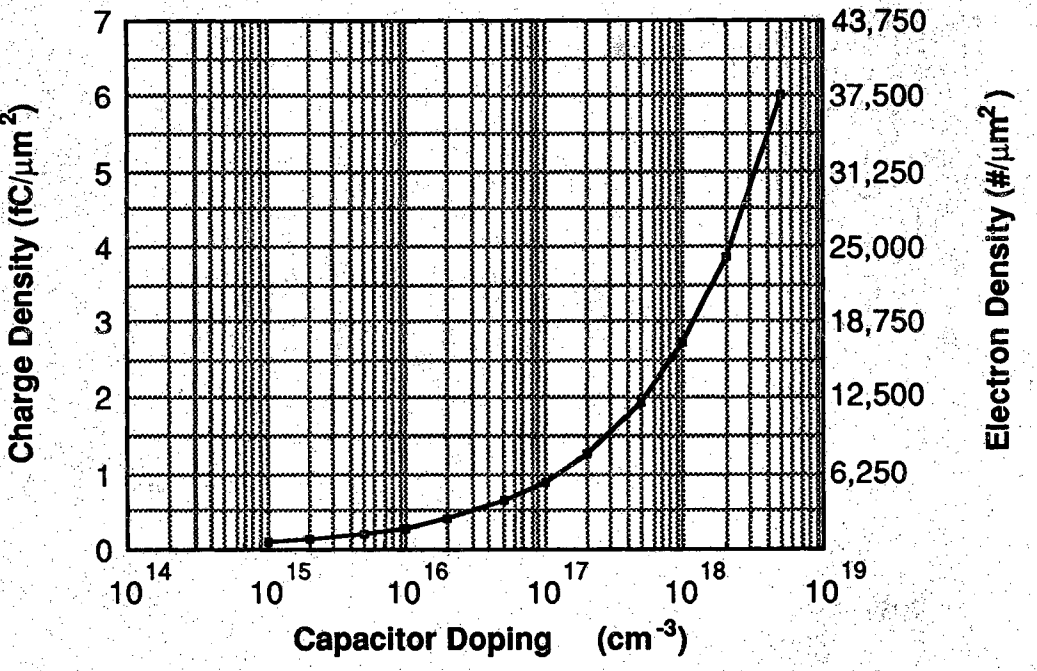


Figure 2.57 Schottky capacitor charge density as a function of doping.

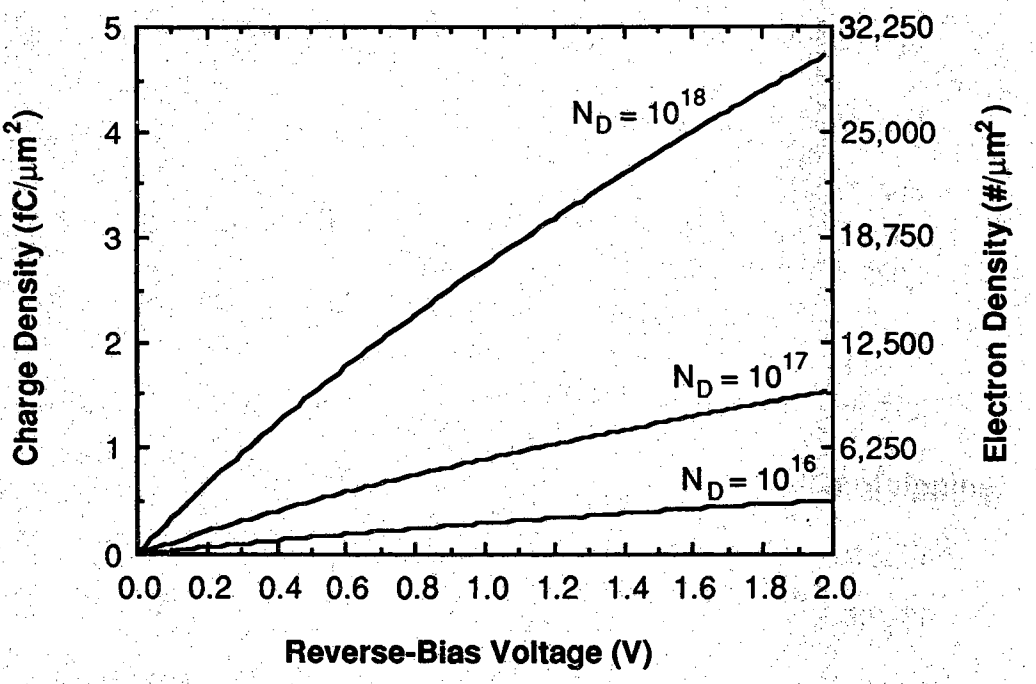


Figure 2.58 Schottky capacitor charge density as a function of voltage.

$$\frac{dQ}{dt} = -I_{RSB} + -I_{RPN} \cong -I_{RSB} \qquad (2.84)$$

Unfortunately the combination of (2.81), (2.83), and (2.84) does not lead to an easily solvable differential equation (c.f. Section 2.3.1 for the PNP capacitor). Instead, the charge decay of the SNP storage capacitor must be analyzed using the numerical techniques as outlined in Section 2.3.5. A simple timestep simulation of equations (2.77), (2.81) and (2.83) can be used to predict the exact form of charge and capacitance recovery transients.

A simple estimation of Schottky barrier capacitor storage time can be obtained from a linear storage time approximation technique similar to that outlined Section 2.3.4. Assuming that 1 V is written to a capacitor based on the Schottky diode of Figure 2.56, the storage time can be estimated by:

$$\tau_S \approx \frac{Q(-1V)\left(1 - \frac{1}{e}\right)}{I_R(-1V)} \qquad (2.85)$$

where Q(-1V) is calculated from (2.77) and (2.83) and I_R(-1V) is calculated from the J-V plot. This calculation produces a worst-case 1/e storage time of 125 mS for the conventional aluminum Schottky barrier of Table 2.7 [16,17]. This storage time barely meets operation requirements for a 1 KHz refresh rate, and access transistor leakages have yet to be accounted for. The above results could have been improved upon by increasing Q(-1V) through heavier doping (Figure 2.57). Clearly however, longer storage times are desirable if GaAs Schottky capacitors are to be used in DRAM arrays.

2.14.3 Ammonium Sulfide Surface Treated Schottky Barriers

The exponential dependence of the Schottky diode saturation current J_S on $\phi_{bn} - \Delta\phi$ suggests that substantial improvements in leakage current

might be obtained by raising the effective barrier height. An increase in barrier height at room temperature as small as 0.1 eV theoretically reduces the reverse leakage current by almost a factor of 50. There have been numerous scientific investigations into the physical nature of GaAs surface pinning, and much progress has been made in recent years [15-22]. The most promising works have centered on the development of various chemical surface passivation techniques, many of which have been shown to significantly improve the electrical characteristics of the GaAs surface [15-22].

Recent work conducted by M. Carpenter et al. [15-17] has shown that pretreating the GaAs surface with ammonium sulfide ($(NH_4)_2S$) before metal deposition can lead to a significant variation in Schottky barrier height with the metal deposited, and this result has subsequently been confirmed elsewhere [18]. Table 2.7 summarizes the results of this work [15-17]. Roughly corresponding to the increase in measured barrier height, the $(NH_4)_2S$-treated diodes that were cooled to near 77K during evaporation exhibit more than a 1000-fold reduction in J_S over their untreated counterparts.

Regrettably, the reverse leakage currents of the treated diodes were below the noise limit of our measurement apparatus. Nevertheless reasonable estimates of reverse leakage characteristics were calculated from forward biased parameters via (2.81), and corresponding 1-V capacitor storage times were estimated from (2.85). Despite the relatively low charge density of the lightly doped GaAs, the theoretical treated Schottky storage times of Table 2.7 are in excess of 6 seconds. This storage time is quite sufficient for use in a DRAM with a 1 KHz refresh clock, and storage times would not be reduced by shrinking sizes due to the fact that both leakage current and charge scale according to device area.

Table 2.7 Theoretical Schottky diode capacitor storage times. The storage time is calculated from measured Schottky diode parameters published in References [16] and [17].

Schottky Diode	J_S (A/cm^2)	$\phi_{bn} - \Delta\phi$ (V)	n	J(-1V) (A/cm^2)	Estimated τ_S (sec)
Untreated Al	1.1×10^{-7}	0.767	1.03	2.0×10^{-7}	0.13
Untreated Au	7.3×10^{-7}	0.781	1.06	6.5×10^{-6}	0.0039
$(NH_4)_2S$ Au	2.1×10^{-9}	0.841	1.08	3.7×10^{-8}	0.68
77K $(NH_4)_2S$ Au	1.8×10^{-10}	0.917	1.09	3.9×10^{-9}	6.46

CHAPTER 3 - ACCESS TRANSISTORS

3.0 Introduction

Just as Chapter 2 covered storage capacitor technologies, this chapter deals exclusively with the development of access transistors suitable for use in GaAs DRAM cells. Since most LSI digital GaAs chips are implemented using JFET- or MESFET-based technologies, this work addresses the use of these technologies as DRAM cell access transistors. Research on other GaAs technologies for use in 1-T DRAM applications is presented elsewhere [124-130].

3.1 Access Transistor Design Goals

The purpose of the DRAM transistor is to provide switched access to the bitline. This simple function is the basis for the two most important access transistor design goals, namely minimization of off current and maximization of on current. Other design considerations, such as transistor area and ease of fabrication, are largely governed by the current state of process technology.

3.1.1 Storage Time - Minimization of Transistor Off Current

When the access transistor is turned off in the DRAM storage state, complete electrical isolation of the capacitor is desired to maximize charge retention. Unfortunately, JFET's and MESFET's are not ideal transistors in which all leakage currents can be completely shut off. Parasitic

transistor leakage mechanisms must be understood and minimized if sufficient DRAM cell storage times are to be obtained. Transistor leakage current issues associated with long-channel JFET's and MESFET's are presented in Section 3.2, while short-channel leakages are discussed in Section 3.3.

3.1.2 Standby Power Dissipation

As outlined in the introduction, another key motivation for undertaking the research outlined in this work is to dramatically cut GaAs memory cell power dissipation. In a DRAM cell, this problem mostly simplifies to the reduction of access transistor off-state leakage currents, even those that do not leak charge stored in the cell. As addressed in Section 3.4, this design consideration is addressed through proper device design and choice of operating voltages.

3.1.3 Access Speed - Maximization of Transistor On Current

High-speed operation is another motivation for the development of a DRAM technology in GaAs. The speed issue is highly complex, involving numerous design tradeoffs in chip architecture, circuit design, and device technology. It must not be overlooked that the speed of a complete RAM chip is as much determined by the speed of addressing, sense-amp, and I/O circuits as it is determined by the speed of the RAM cells themselves. Clearly though, a high speed RAM chip must consist of high-speed RAM cells. Since DRAM cell read/write operations are based on the movement of charge between the capacitor and the bitline, the fastest cell is one that moves the charge in the shortest time. It is therefore desirable that the turned-on access transistor carry as much current as possible during read/write operations.

3.1.4 Other Transistor Considerations

Consistent with the desire to minimize DRAM cell area, it is obviously beneficial to minimize the area of the access transistor. Shrinking FET sizes are largely driven by improvements in lithography and other process technologies which are not covered in this work.

The attractiveness of a GaAs dynamic RAM technology would be greatly enhanced if it could be manufactured based entirely on standard processes already in widespread use. Since most LSI GaAs IC's rely on high-yield planar ion-implanted FET's, it would be advantageous to develop cells that could be implemented in these technologies. Most of the experiments presented in this work are based on layers grown and doped by epitaxial methods. However, since these epitaxial devices are simple JFET's and MESFET's, most of the device concepts presented can be translated to the appropriate ion-implanted GaAs FET technology.

3.2 Long-Channel Access Transistor Leakage

The performance of the GaAs DRAM cell in the idle storage state is largely determined by the off-state characteristics of the access transistor. Parasitic leakage currents from the turned-off access transistor can seriously affect DRAM cell storage times and standby-state power dissipation. This section presents a detailed theoretical and experimental discussion of off-state transistor leakages in long-channel GaAs JFET's and MESFET's, and puts forth methods for reducing these parasitics.

Of paramount importance to DRAM cell storage time is the drain leakage of the access transistor. Figure 3.1 depicts an N-channel FET-accessed DRAM cell with a logic one stored on the capacitor. The positive charge on the capacitor is isolated from the grounded bitline by the turned-off access transistor. However, the parasitic FET drain leakage currents shown in the figure will discharge the capacitor causing the positive charge to decay over time. By minimizing the off-state drain current of the FET access transistor, cell storage time can be maximized and overall DRAM chip refresh requirements can be relaxed.

For a doped-channel FET to be considered a long-channel device, the channel potential must be primarily controlled by the gate. This makes the threshold voltage independent of drain voltage so that $V_T = V_{T0}$ [32]. These conditions are largely satisfied for GaAs doped-channel FET gate lengths greater than 1.5 μm, provided the selected operating voltages are reasonable (2 V or less).

The two sources of FET off-state drain leakage are drain-to-source current I_{DS} and drain-to-gate current I_{DG} (Figure 3.1). The role that these two components play is best understood through the MESFET subthreshold current characteristic of Figure 3.2. This plot shows the drain current I_D (on a logarithmic scale) as a function of gate voltage V_G for a constant drain bias V_{DS} = +0.5 V. The source and substrate are both held at system ground. The threshold voltage V_{T0} for this particular N-channel device is about 0.1 V. Above threshold ($V_G > V_{T0} = 0.1$ V) the turned-on MESFET carries an abundance of source-to-drain current.

3.2.1 Drain-to-Source Leakage

When the gate is taken below threshold ($V_G < V_{T0} = 0.1$ V), the reverse-biased gate depletes the entire N-doped channel. This does not entirely switch off I_{DS} however, as electrons from the source diffuse through depleted areas to the positively biased drain. This phenomenon, known as source-to-drain subthreshold conduction, is an extremely complex and important topic of current research [28-31]. Roughly speaking (see Section 3.3 for a more accurate description) the subthreshold transport of majority carrier electrons from source to drain occurs through a combination of thermionic emission and diffusion, somewhat analogous to current transport in Schottky barriers. The potential barrier that carriers from the source must overcome to reach the drain increases as the gate bias is taken more negative, as depicted in 1-D by Figure 3.3. The current is exponentially dependent on the potential barrier ϕ_b,

$$I = I_0 e^{-q\phi_b/kT} \qquad (3.1)$$

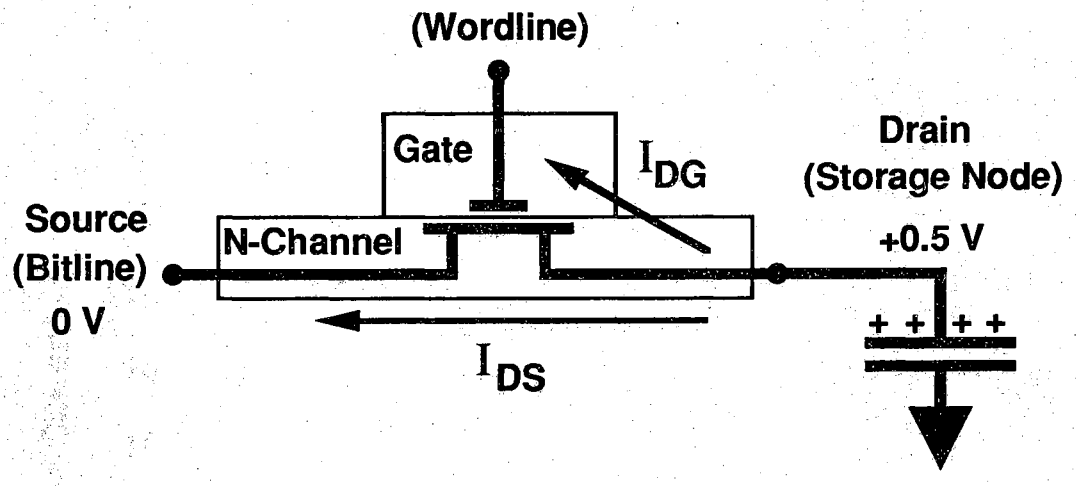


Figure 3.1 Doped-channel FET off-state leakage currents. The parasitic leakages will discharge stored data in the DRAM cell.

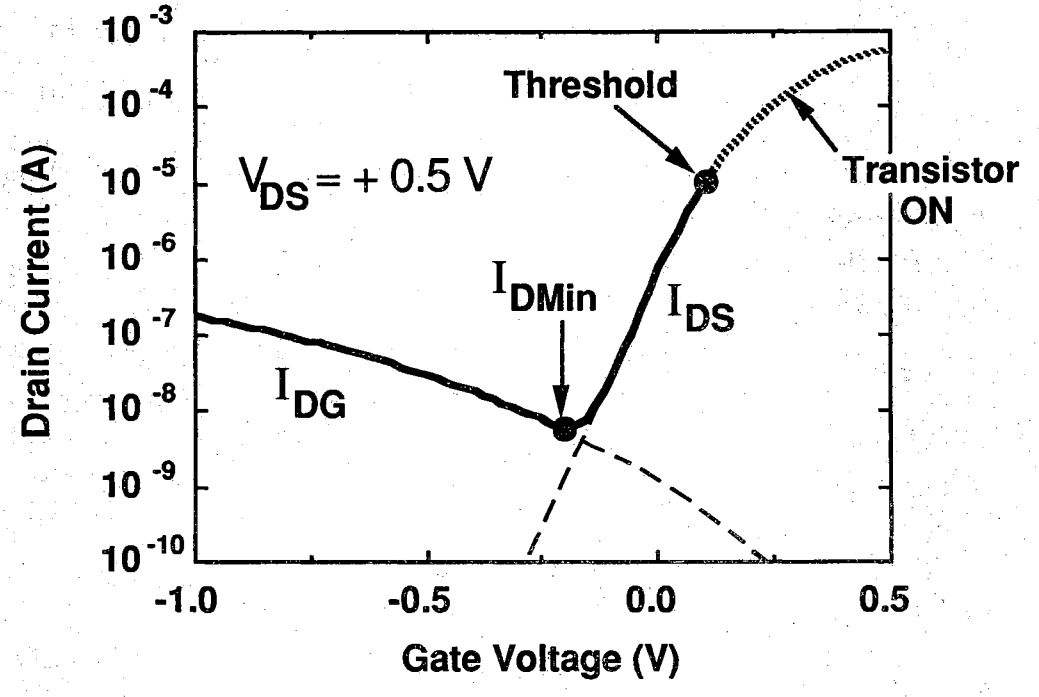


Figure 3.2 Doped-channel GaAs FET subthreshold leakage current characteristic. To maximize DRAM cell storage time the device should be biased at $V_G = V_G(I_{DMin})$. This characteristic was taken from a 10 x 350 μm^2 ring-gate MESFET.

so the subthreshold source-to-drain conduction declines exponentially with increasingly negative gate voltage [30]:

$$I_{DS} = I_{DSSub0}\left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right]\exp\left(\frac{q}{n_{Sub}\,kT}(V_{GS} - V_{T0})\right) \quad (3.2)$$

I_{DSSub0} is the current measured at threshold ($V_G = V_{T0}$), and n_{Sub} is the subthreshold ideality factor. The term in the square brackets simplifies to unity for any appreciable $V_{DS} > 0.1$ V, so it is essentially irrelevant to the DRAM access transistor leakage problem. An $n_{Sub} = 1.0$ represents the ideal case that the change in gate potential translates 1:1 into a change in channel potential, thereby causing I_{DS} to change by a factor of $e^{q\Delta V_G/kT}$. An equivalent expression for the I_{DS} subthreshold current given in (3.2) is:

$$I_{DS} = I_{DSSub0}\, 10^{(1/S_{Sub})(V_G - V_{T0})} \quad (3.3)$$

where S_{Sub} is defined as the subthreshold slope. The subthreshold slope represents the gate voltage swing required to change I_{DS} by a factor of 10, and is extracted from the linear slope (measured in volts/decade) of the $\log_{10}$ plot of I_{DS} versus V_G (Figure 3.2). The subthreshold slope S_{Sub} is related to n_{Sub} by:

$$S_{Sub} = \frac{kT\, n_{Sub}}{q}\ln(10) \quad (3.4)$$

At room temperature (300 K), the ideal subthreshold slope corresponding to $n_{Sub} = 1.0$ is $S_{Sub} = 60$ mV/decade.

3.2.2 Gate Leakage

In a long channel device, the total drain current I_D drops exponentially with V_G until I_{DG} becomes significant (Figure 3.2). The operating point at which I_D reaches its minimum value is referred to as the

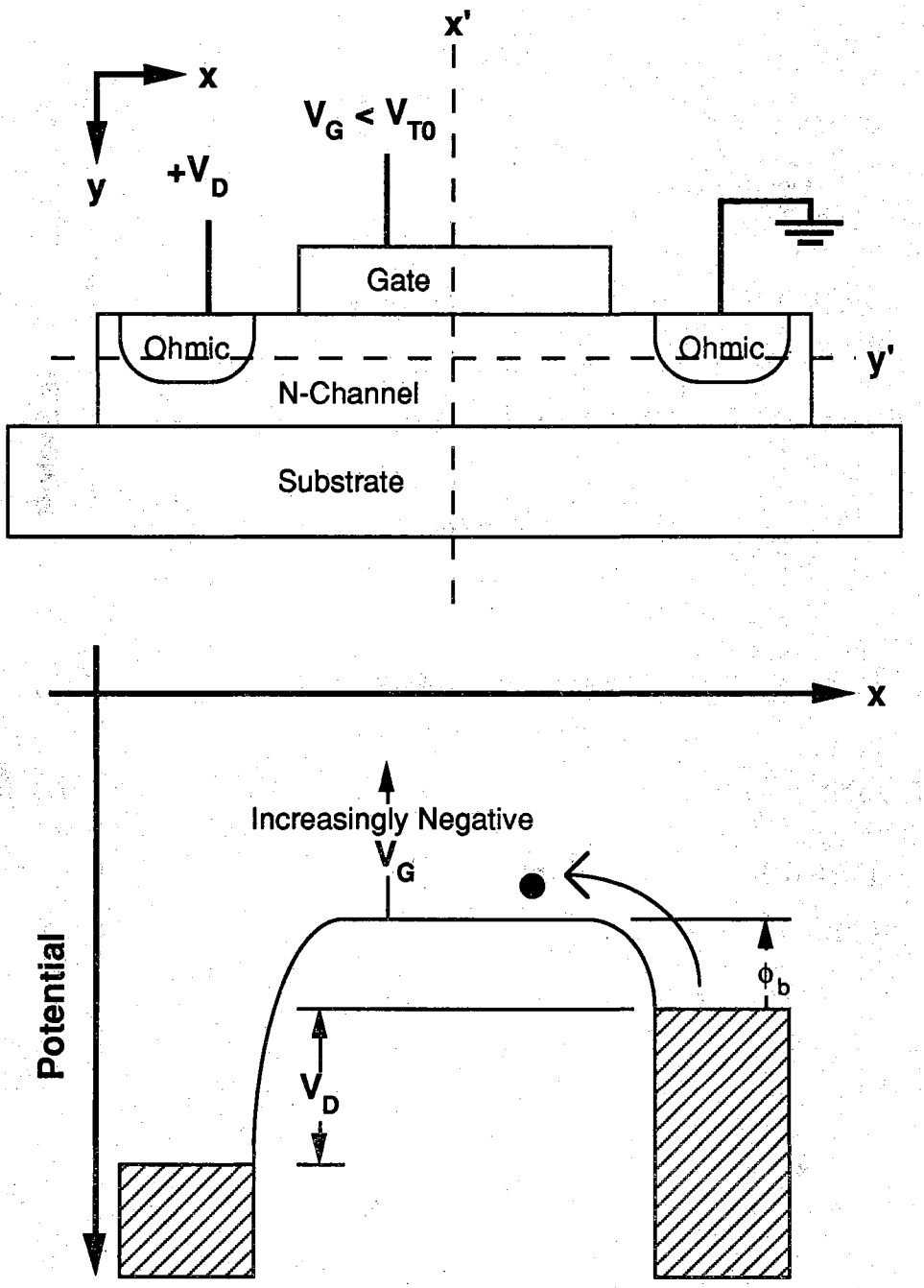


Figure 3.3 Subthreshold drain-to-source conduction in doped long-channel FET's. The gate controls the mid-channel potential along x = x' thereby controlling the potential barrier ϕ_b that source electrons must surmount to reach the drain. The potential diagram is taken along y = y'.

subthreshold current minimum I_{DMin}. The operating region in which I_{DG} is the dominant leakage mechanism ($V_G < V_G(I_{DMin})$) is referred to as the gate-diode-limited subthreshold regime.

I_{DG} is the current between the negatively biased gate and the positively biased N-drain region, which actually is nothing more than the reverse-biased leakage of the gate-to-drain diode. The drain current minimum I_{DMin} of a long-channel FET is thus determined by the gate diode leakage. Because it has a Schottky gate, the same thermionic emission mechanisms presented in Section 2.14 limit the current minimum of a MESFET. Similarly, I_{DMin} of a long-channel JFET is determined by the same PN junction thermal generation leakage mechanisms that were discussed in most of Chapter 2.

In cases where I_{DG} changes rapidly with V_G (e.g., Figure 3.2), the choice of device threshold voltage can seriously affect I_{DMin}. Had the threshold voltage of the device in Figure 3.2 been around -0.5 V, I_{Dmin} would've occured near V_G = -1.0 V; the corresponding increase in V_{DG} would've meant a greater than 10-fold increase in the apparent subthreshold current minimum.

3.2.3 Direct Comparison of JFET and MESFET Leakages

To experimentally compare the leakage characteristics, the epitaxial JFET and MESFET cross-sections of Figures 3.4 and 3.5 were fabricated using procedures outlined in the Appendices. A large W_{Gate} = 350 μm ring-gate FET structure (Figure 3.6a) was used as a basis of comparison, with the difference in gate length being a factor of 2 (JFET L_{Gate} = 5 μm, MESFET L_{Gate} = 10 μm). Figure 3.7 shows the measured subthreshold current characteristics of the JFET and MESFET structures on the same axis. The PN junction gate JFET exhibits almost a 1000-fold smaller I_{DMin} than the Schottky gate MESFET which cannot be attributed to the difference in V_{DG}. This difference reflects the low-leakage superiority of PN junctions over conventionally prepared Schottky barriers in GaAs (Section 2.14). These results imply JFET-based DRAM technologies will have longer storage times than conventional MESFET-accessed approaches.

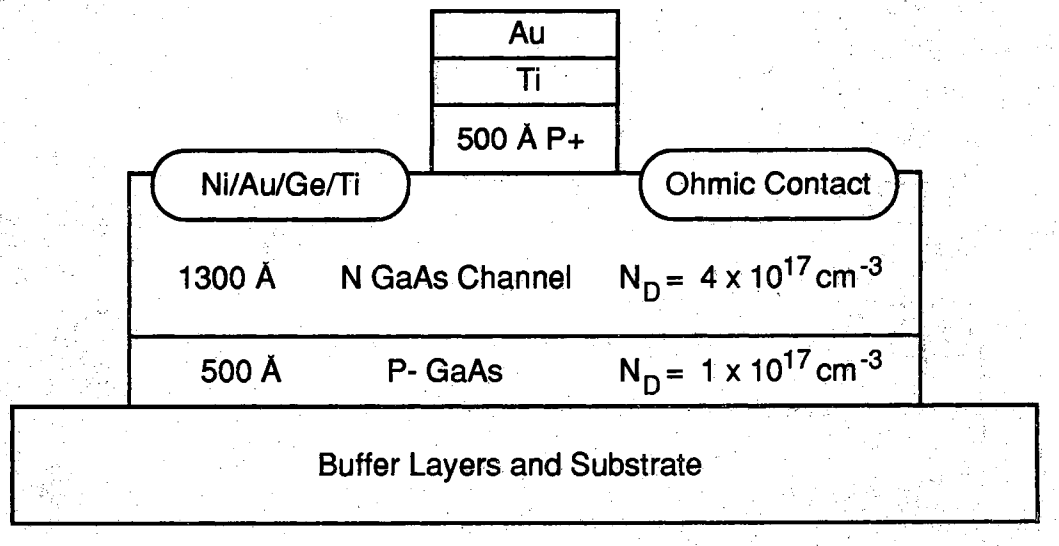


Figure 3.4 Epitaxial JFET cross-section. The processing sequence was gate metal definition, mesa etch, P^+ cap removal etch (i.e., N-channel surface exposure etch) self-aligned to the gate metal, and ohmic contact deposition and alloy (Appendix 2).

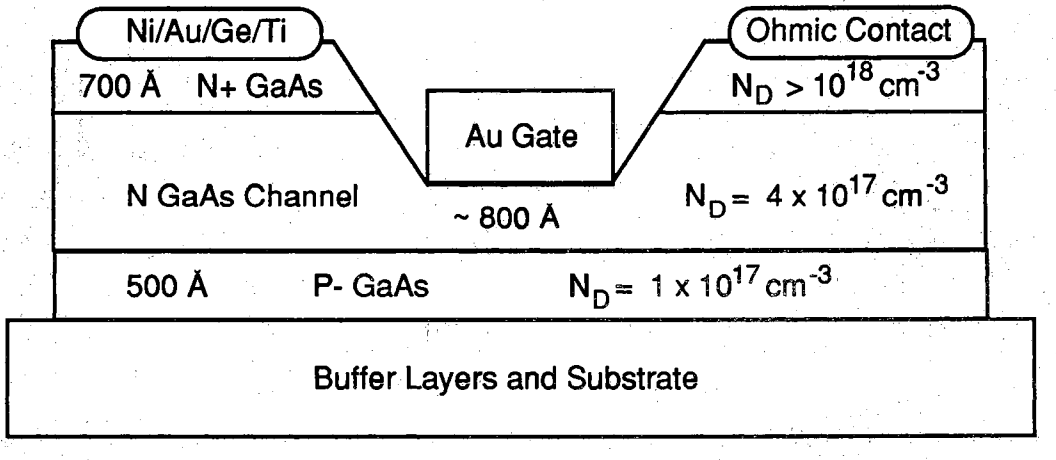
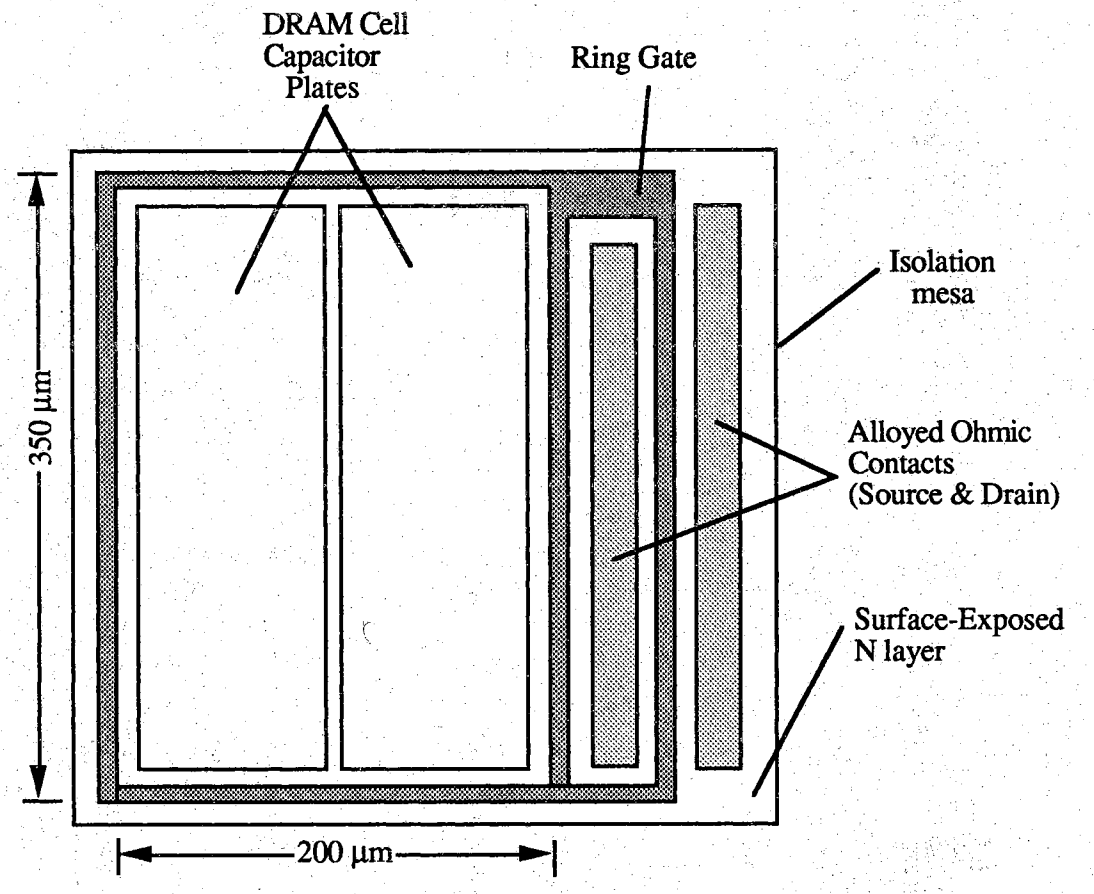
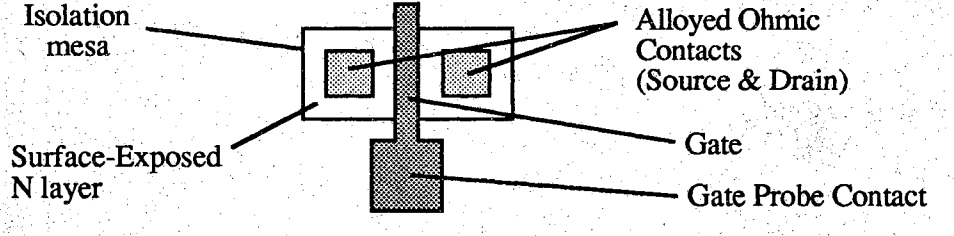


Figure 3.5 Epitaxial MESFET cross-section. The processing sequence was mesa etch, ohmic contact deposition and alloy, and gate recess-etch and gate deposition patterned by the same mask (Appendix 1).



a) Large ring-gate FET/DRAM cell



b) Conventional non-ring-gate FET

Figure 3.6 Epitaxial FET test structure layouts. The ring-gate structure in (a) combines a test FET and a test DRAM cell on the same mesa.

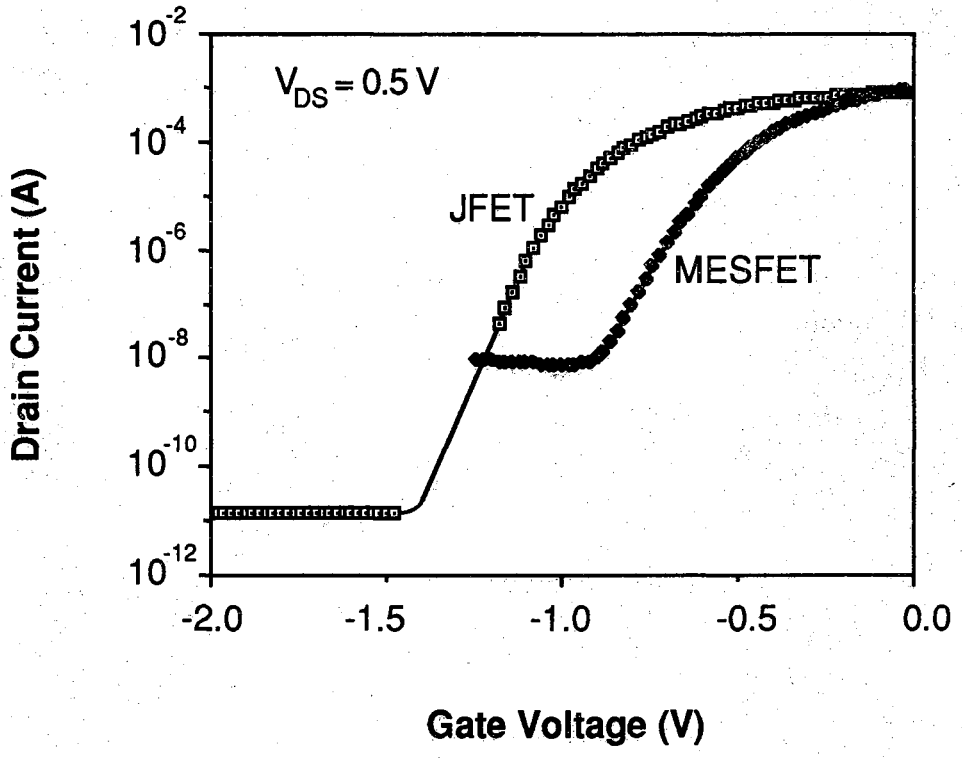


Figure 3.7 Comparison of JFET and MESFET transistor turn-off characteristics. The increased MESFET leakage is due to thermionic emission of electrons over the Schottky gate potential barrier, whereas the JFET PN junction gate leakage is limited by thermal generation. The layout of the devices compared is given in Figure 3.6a, with JFET L_{Gate} = 5 μm and MESFET L_{Gate} = 10 μm.

3.2.4 Reduced MESFET Leakage Through $(NH_4)_2S$-Treated Gates

The subthreshold drain current minimum of a long channel MESFET could be reduced if the reverse biased Schottky gate diode conduction (I_{DG} of Figures 3.1 and 3.2) were diminished [29,30]. The primary source of current in GaAs Schottky barriers is thermionic emission of carriers over the junction potential barrier (Section 2.14). By fabricating GaAs MESFET's employing the $(NH_4)_2S$-technique of Section 2.14.3 to increase the barrier height of the Schottky gate, a remarkable reduction gate-diode-limited MESFET subthreshold current was obtained.

The complete fabrication procedure for the MESFET structure of Figure 3.5 is outlined in Appendix 1, but the application of $(NH_4)_2S$-treated gates is detailed here. Wafers with the gate pattern already defined in 4% PMMA resist were soaked for 2 minutes in a saturated $(NH_4)_2S$ solution, DI rinsed, blown dry. The teated wafers along with untreated control samples were then placed into a vacuum system, and Au gates were thermally evaporated with the wafers cooled to near 77 K by circulating LN_2 through the substrate holder. To minimize defect-forming surface chemical reactions, the processing from the treatment to pumpdown of the evaporation system was carried out without delay, and use of excited electron sources (e.g., electron beams and ionization gages) was explicitly avoided [15-17,27,28].

Figure 3.8 shows the measured drain and gate currents of typical $(NH_4)_2S$-treated and untreated 10 x 350 μm^2 ring-gate MESFET's (layout in Figure 3.6a) as a function of gate voltage with V_{DS} = 0.5 V. The $(NH_4)_2S$-treated gate MESFET's exhibited a greater than 100-fold reduction in subthreshold current minimum I_{DMin} over their untreated counterparts. This decrease is directly attributable to the reduction in leakage current of the ammonium sulfide treated Schottky gates. To our knowledge, the current density of the subthreshold current minimum (in terms of both current/gate area and current/channel width) is the lowest ever reported in a GaAs MESFET [28-31,33-36]. Aside from the reduction in subthreshold current, there were no discernable differences between the measured electrical characteristics of treated and untreated MESFET's.

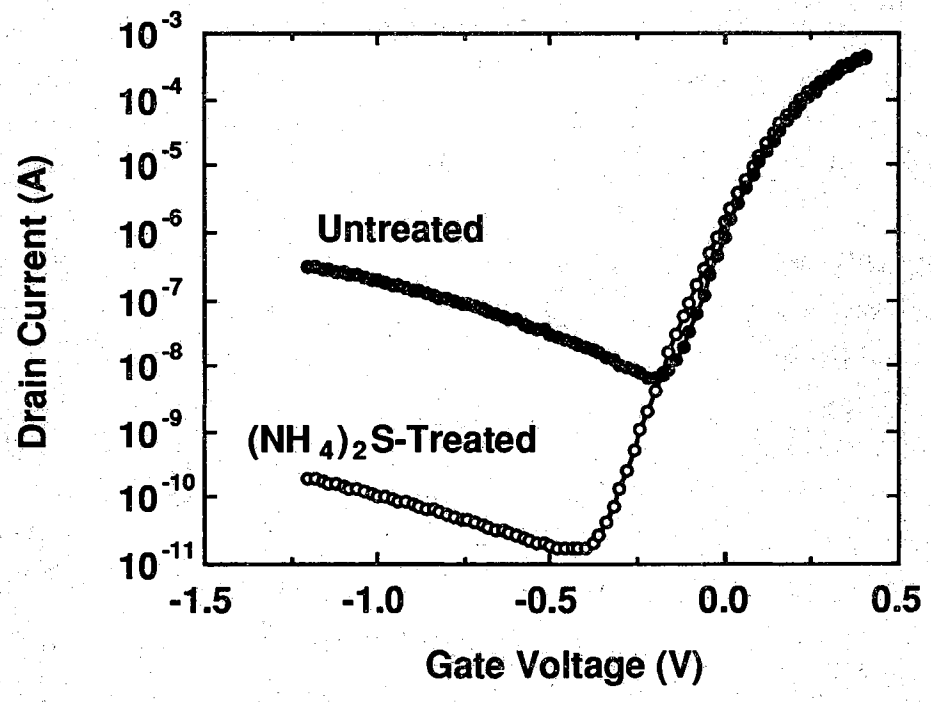


Figure 3.8 Comparison of $(NH_4)_2S$-treated gate and conventional gate MESFET subthreshold current characteristics. The 10 x 350 μm^2 structure of Figure 3.6a was used on the device cross-section of Figure 3.5, and the drain-to-source voltage is 0.5 V.

The electrical characteristics have remained stable for over a year during undessicated storage at room temperature, despite the absence of passivation layers. This technique shows promise for use with gate materials other than gold, provided deposition techniques and gate-to-semiconductor work function differences are optimized. As no exotic in-situ processing is required, the technique is suitable for use in large-scale integrated circuits such as high-density DRAM's.

3.2.5 Drain Diode FET Leakage

Although Figure 3.1 depicts the two most well-known sources of transistor leakage (I_{DS} and I_{DG}), the simplified schematic FET overlooks the existence of substrate leakage mechanisms. A more accurate representation of an integrated circuit FET including the substrate is given in Figure 3.9. For speed purposes, most GaAs IC FET's are fabricated on semi-insulating starting material to minimize parasitic substrate capacitances. As in Figure 3.1, the drain is biased to + 0.5 V and the source is grounded. However, the presence of insulating material does not completely eliminate the flow of current between the positive drain and the grounded substrate, resulting in a third parasitic drain leakage mechanism I_{DSub}.

Since most unintentionally doped GaAs material is p-type in nature, a P^-N junction diode is effectively formed with the drain. This junction is exactly the same as the lower junction of the non-symmetric P^+NP^- storage capacitors discussed in Section 2.12. Depending on the substrate acceptor concentration, the junction depletion will extend deep into the substrate, and thermal generation of electron-hole pairs will take place in the reverse-biased depletion region resulting in leakage current.

3.2.5.1 Alloy Contact Drain Diode Leakage

Depending upon the ohmic contact process employed during FET fabrication, the drain-to-substrate diode may not in fact be dominated by

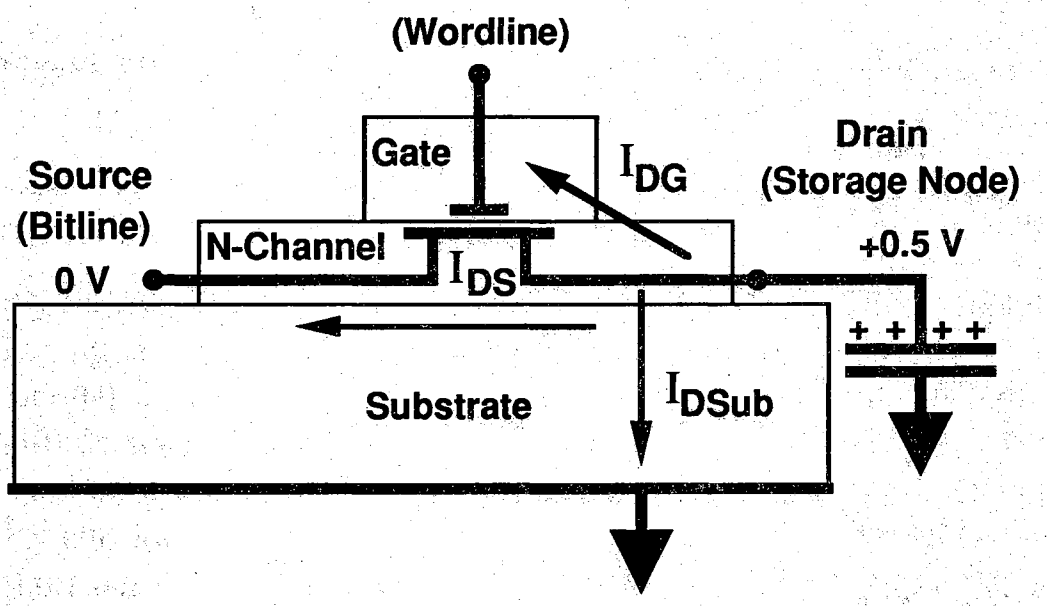


Figure 3.9 FET drain subthreshold leakage sources including drain-to-substrate leakage.

PN junction physics. There are numerous recipes for the formation of low-resistance ohmic contacts to n-type GaAs. Most of these involve a thermal annealing procedure in which part of the ohmic metallization diffuses somewhat into the semiconductor. There are often cases where the ohmic contact spikes far into the semiconductor, beneath the metallurgical PN junction as depicted in Figure 3.10. This condition does not completely short out the drain diode junction. Each spike can be viewed as a tiny rectifying Schottky barrier to the lightly doped semiconductor, and the insulating material provides a series resistance to the grounded substrate.

In cases where sufficient spiking had taken place, the electrical characteristics of the drain-to-substrate diode were dominated by the spiked contact metal instead of the PN junction. I-V measurements conducted on various test structures revealed that spiking was present on almost every wafer fabricated during these experiments, though JFET's were generally more afflicted than MESFET's. Because ohmic contact quality is highly

process dependent, spiking may not be a problem in FET's fabricated elsewhere.

The drain diode leakage was large enough in some FET's that it played a significant role in the measured drain leakage characteristics. The measured JFET leakage characteristic of Figure 3.11 is one such example. The drain current minimum of this device is not limited by gate-to-drain leakage as outlined in Section 3.2.2, but is instead determined by drain-to-substrate leakage. This fact was established through several experimental observations. The drain current does not increase as V_G is taken negative beyond the current minimum, indicating that the bias on the dominant leakage mechanism is not changing with gate voltage. Since the drain-to-substrate bias is constant at 0.5 V while V_{GD} varies with gate bias, this immediately suggests that the drain diode is responsible for the apparent current minimum. Second, the observed current minimum is consistent with measurements of drain-to-substrate diode testers on the wafer. Finally, measurements of the gate-to-channel diode (lower curve of Figure 3.11) and related test structures revealed that I_{DG} was approximately 100 times smaller than the measured drain current minimum.

If a spiked ohmic drain contact were incorporated into an overall DRAM cell, the storage time effects would most likely be catastrophic. The P^+NP^- capacitors of Section 2.12, whose bottom junctions are similar to the drain-to-substrate diode of a JFET or MESFET, showed storage times of a few seconds. Given the above experimental results, the increase in leakage current from the ohmic contact spiking would most likely decimate DRAM cell storage times (Figure 3.10).

It is believed the spiking problem can be eliminated with an improved ohmic contact process; however, a simpler solution is to get rid of the drain ohmic contact metallization altogether. The directly-connected diode capacitor cells of Chapter 4 realize this concept, and the spiking problem is rendered obsolete in DRAM cells of this type. For these reasons the spiking leakage will be removed from further consideration as a factor limiting DRAM cell storage time. However, the parasitic spiking leakage could pose problems to the development of non-directly connected cells. Furthermore as witnessed by the characteristics of Figure 3.11, it interferes with the accurate measurement of FET draincurrent minimums.

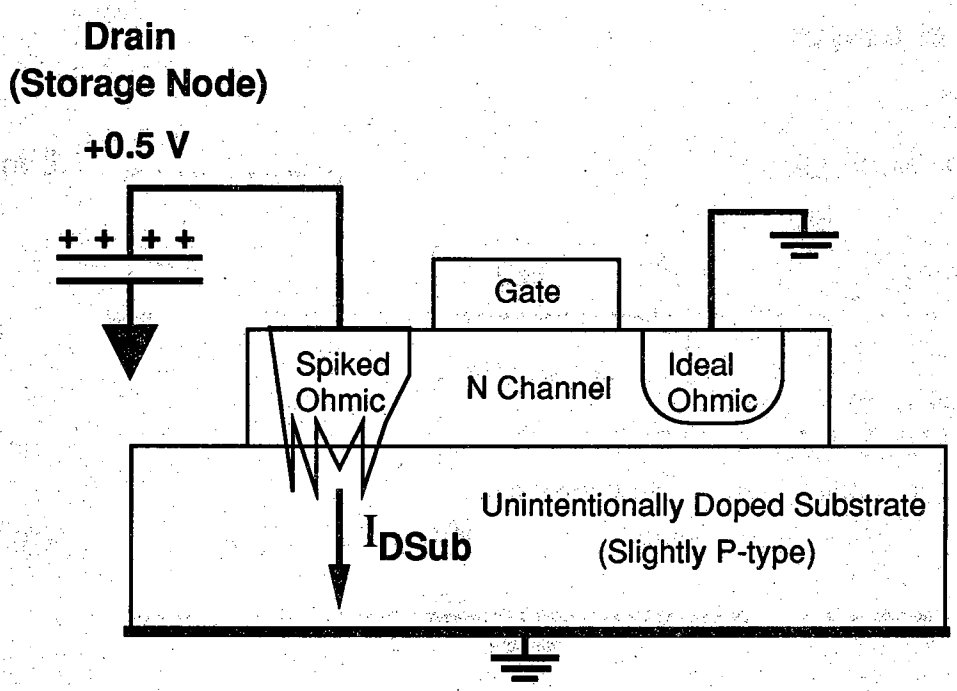


Figure 3.10 Excess drain leakage caused by alloy contact spiking. The extra current could kill DRAM cell storage times.

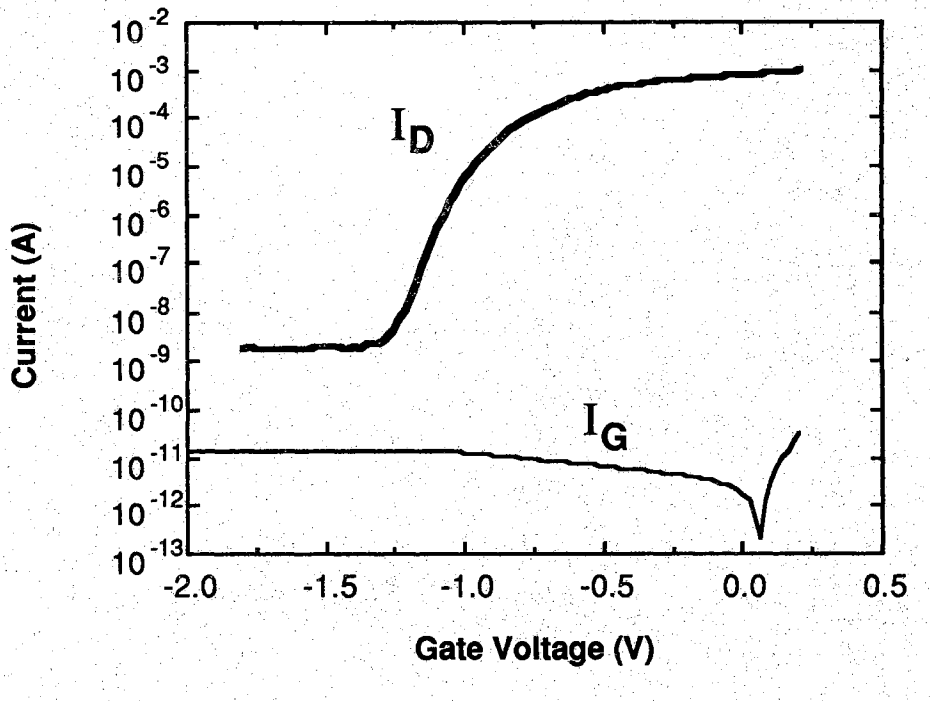


Figure 3.11 Effect of spiked drain contact on measured JFET subthreshold drain current characteristics. The spiked drain diode (Figure 3.10) determines the drain current minimum. This 5 x 350 μm^2 device had the layout given in Figure 3.6a.

For this reason most of the JFET drain current minimums presented in this work were determined from gate diode characteristics, and are not directly measured drain currents. In the absence of drain-to-substrate leakage, the gate-to-drain diode ultimately determines the leakage performance of the long-channel FET. Aside from a few differences, these gate leakages roughly amount to the reverse-biased diode leakages that were detailed in Chapter 2.

3.2.6 Experimental Long-Channel JFET Subthreshold Leakage

Proper analysis of experimental JFET and MESFET leakage currents requires careful consideration of device geometries and non-obvious parasitic device leakages. The JFET cross-sections of Figure 3.4 were investigated, and fabrication procedures are outlined in Appendix 2. Figure 3.12 shows the measured V_{DS} = 0.5 V subthreshold drain characteristics of a 5 x 350 μm^2 ring gate JFET (Figure 3.6a) at 25, 44, and 85° C. Excessive drain diode spiking leakage dictated that current minimums be measured separately using the gate diode (c.f. Figure 3.11). As expected for a long-channel device, the threshold voltage of -1.0 V was not a function of drain bias below V_{DS} = 2 V. The subthreshold ideality factors fell between 1.1 and 1.3, and I_{DMin} resided somewhere between V_G = -1.4 to -1.5 V for the temperature range tested.

The examination of non-ring-gate JFET's provided some valuable information on parasitic leakages. These transistor leakages are often overlooked because they have little effect on conventional FET IC's, but in a DRAM process requiring very low access transistor leakages they could devastate cell storage times. In the first JFET processing run, device mesas were defined prior to gate metallization resulting in the device structure of Figure 3.13a. The drain current minimums of small non-ring-gate devices (Figure 3.6b, W_{Gate} = 25 μm, 1 $\mu m < L_{Gate} <$ 10 μm) were noted to be larger than I_{DMin} for the huge 5 x 350 μm^2 ring-gate device (Figure 3.6a). The disparity was due to tiny Schottky diodes formed between the the N-channel mesa sidewall and the gate metallization (Figure 3.13a). The problem was corrected in subsequent JFET runs by patterning gates prior

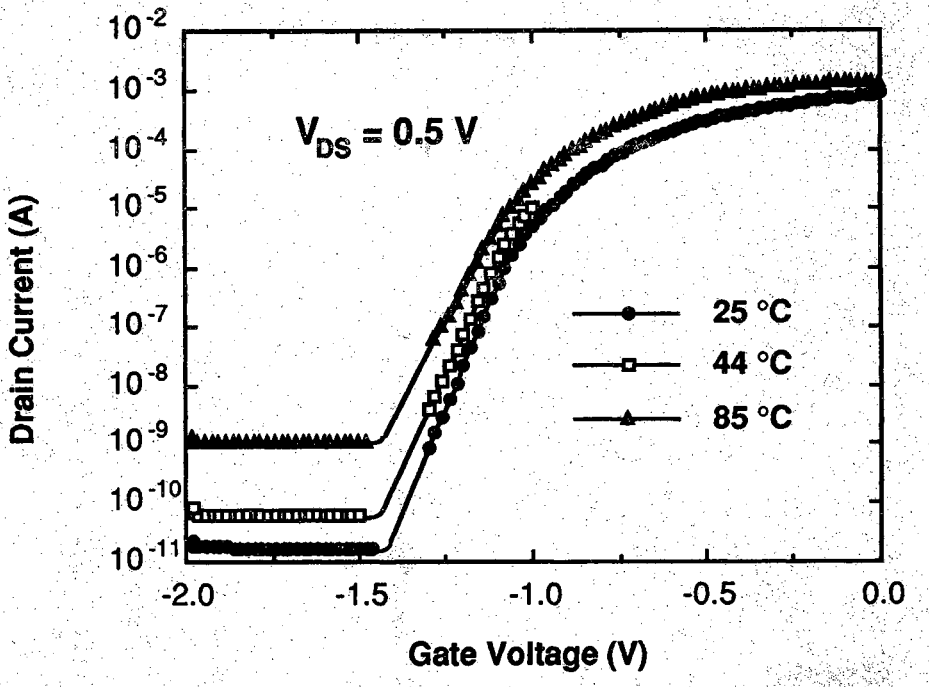
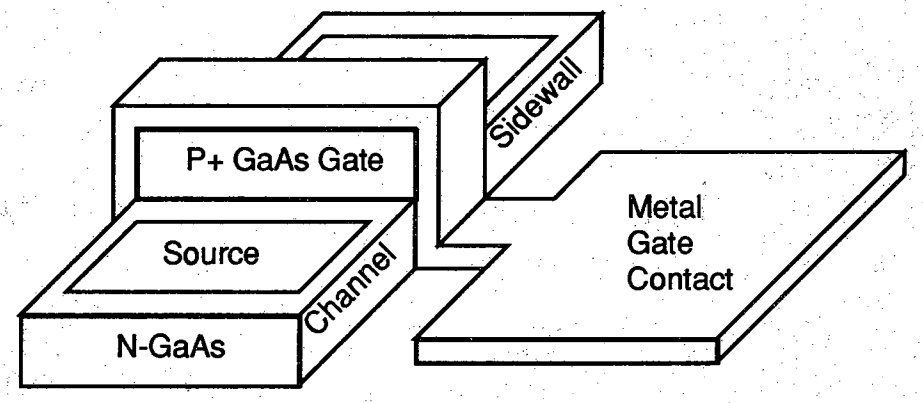
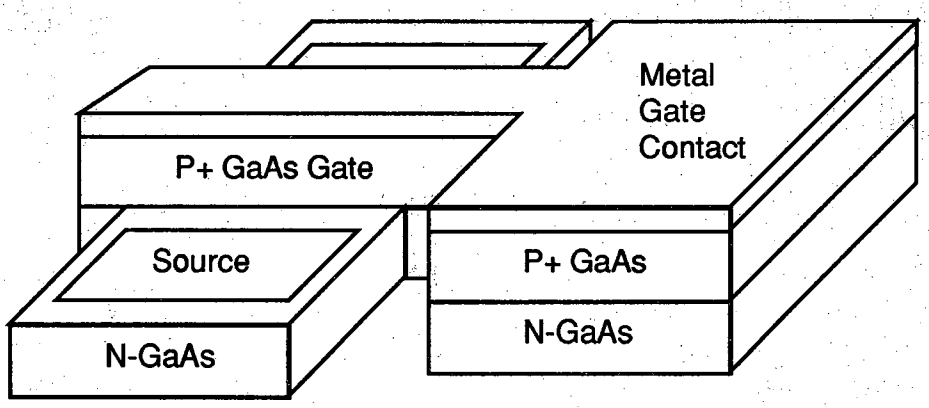


Figure 3.12 5 x 350 μm^2 ring-gate JFET subthreshold current characteristics at three different temperatures.



a) JFET with parasitic sidewall Schottky diodes



b) Corrected epitaxial non-ring-gate JFET

Figure 3.13 Conventional epitaxial JFET structures. Device a) showed excessive gate leakages due to parasitic Schottky diodes formed between the channel sidewall and the gate metallization.

to the mesa definition, producing the non-ring-gate device structure shown in Figure 3.13b.

A direct characterization of I_{DMin} as a function of JFET gate dimensions would have been useful, as it might verify the gate diode scaling dependences predicted by the PN junction physics of Chapter 2. However, parasitics from the large gate probe contact in Figure 3.13 and spiked drain diodes prevented the accumulation of meaningful data regarding this subject. An in-depth analysis of ring-gate JFET leakage is left to Chapter 4, where direct comparisons to PNP capacitor leakages are drawn.

3.2.7 Experimental Long-Channel MESFET Subthreshold Leakage

The MESFET cross-section of Figure 3.5 were fabricated using the process outlined in Appendix 1. The approach relied on a wet recess-etch to define the doped-channel thickness under the gate, so etch-rate nonuniformities caused inter-wafer threshold variations of a few tenths of a volt. The leakage characteristics of a conventional (untreated) 10 x 350 μm^2 ring-gate MESFET's (Figure 3.6a) are given in Figure 3.14. The gate leakage is much larger that the drain diode leakage, so measured drain current minimums are consistent with measured gate currents. It is interesting to note that $V_G(I_{DMin})$ changes little with temperature.

Due to parasitic leakages associated with non-ring-gate structures, consistency between I_G and I_{DMin} was only observed in the ring-gate structure. As depicted in Figure 3.15, the gate metallization which lies off the mesa effectively forms a P-type Schottky diode to the substrate. The application of negative gate bias to turn-off the N-channel MESFET produces a forward-bias on the parasitic diode to the grounded substrate. Although the resulting current flow is limited by the highly resistive substrate, Figure 3.16 shows that it is several orders of magnitude larger than the drain current minimum. An insulating dielectric placed between the gate contact and the substrate would help the situation, but the parasitic cannot be completely eliminated due to gate-mesa overlap requirements.

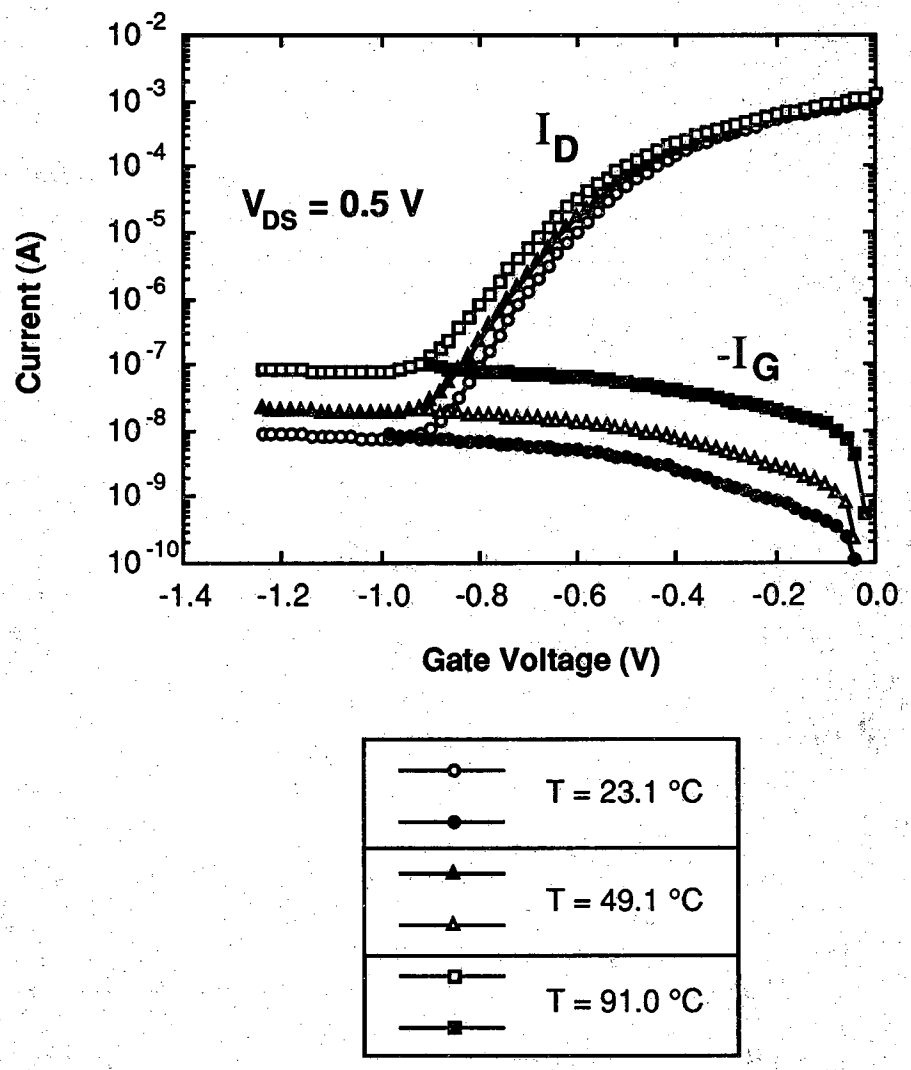


Figure 3.14 Conventional 10 x 350 μm^2 ring-gate MESFET subthreshold current at three different temperatures. The gate-to-channel leakage is larger than the drain-to-substrate leakage, so the drain current minimum corresponds to the measured gate current.

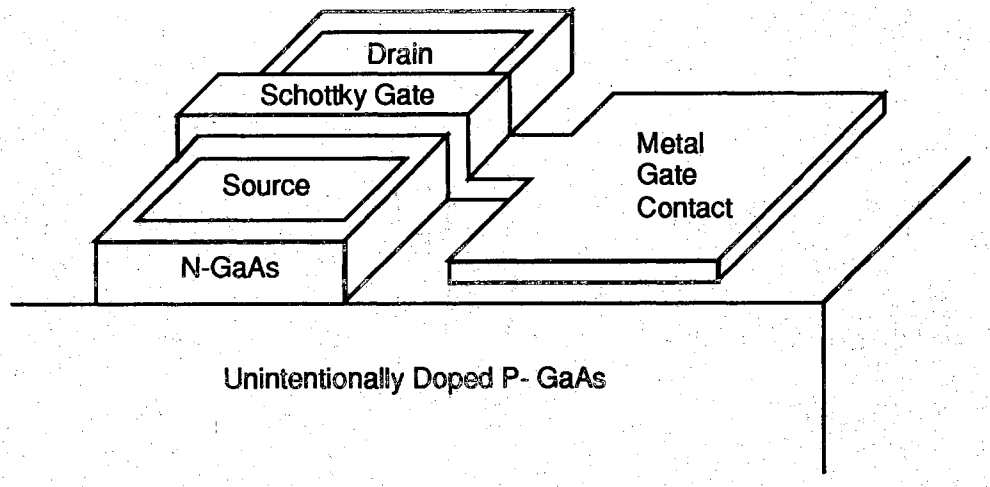


Figure 3.15 Epitaxial MESFET with large parasitic gate probe contact. Even if the probe contact were eliminated, a parasitic diode would exist where the gate overlaps the edge of the mesa.

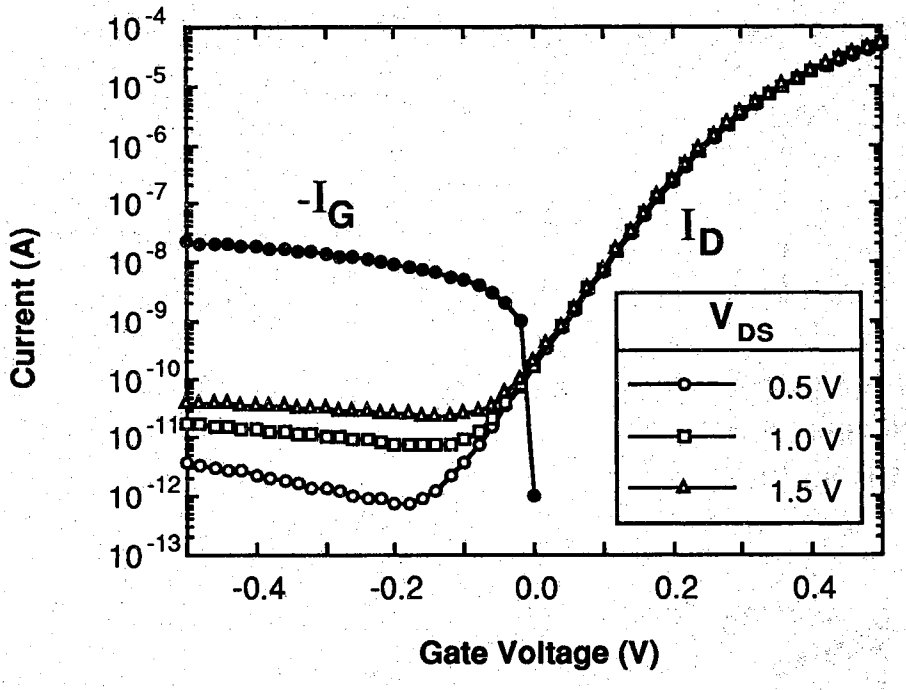


Figure 3.16 Room-temperature subthreshold leakage performance of a 5 x 30 μm^2 non-ring-gate MESFET. The excess gate current arises from the off-mesa gate probe contact of Figure 3.15.

The large gate contact was also responsible for some discrepancies in measured subthreshold slopes. The large current drawn by the gate contact changes the potential of the GaAs regions encompassing the doped channel. The result is a backgating effect, whereby the channel is pinched-off from both sides as V_G swings negative. Lacking any off-mesa contacts, ring-gate devices are gated only from the top, and thus exhibit higher subthreshold slopes. The subthreshold slope in Figure 3.16 for the 5 x 30 μm^2 non-ring-gate device is very nearly ideal at 60 mV/dec (n_{Sub} = 1.02), while 10 x 350 μm^2 ring-gate devices on the same wafer exhibit more realistic slopes near 70 mV/dec (n_{Sub} = 1.19).

3.3 Short-Channel Access Transistor Leakage

As gate lengths shrink into the submicron regime, the electric influence of the source/drain regions becomes increasingly important. Due to the close proximity of the source and drain, the mid-channel electric potential is no longer solely determined by the gate; it is significantly affected by the source/drain potentials. This leads to what are appropriately called short channel effects in FET's [1,29-36]. Figure 3.17 pictorially demonstrates the fundamental nature of the short-channel problem. With the source and substrate grounded, the positively biased drain is close enough to the source that it's electrical influence extends over the channel length.

3.3.1 Threshold Voltage Dependence on Drain Bias

Despite the use of identical channel doping profiles, short-channel phenomena cause differences in the turn-off characteristics of short-channel FET's from their long-channel counterparts. The potential on the drain affects the entire short-channel, resulting in the threshold voltage V_T becoming a function of drain bias [1,29,30,32]. In doped-channel GaAs FET's, the threshold voltage is linearly dependent on drain voltage [30]:

$$V_T = V_{T0} + \kappa V_{DS} \qquad (3.5)$$

where $\kappa < 0$ is the drain bias threshold shift coefficient, and V_{T0} is the threshold voltage at zero drain bias. It should be noted that κ is an empirical constant unique to a specific FET doping profile and gate length, and that $\kappa = 0$ corresponds to the long-channel device situation.

3.3.2 Physics of Short-Channel FET I_{DS} Leakage

Though valid for long channel FET's, the crude explanation of leakage I_{DS} presented in Section 3.2.1 masks the extremely complex nature of source-to-drain subthreshold conduction. The potential barrier ϕ_b that electrons must traverse to get to the drain is actually a two-dimensional function of position. Just as gate voltage affects the channel potential, voltages at the source and drain also affect the device electrostatics. The source/drain influences are not important to I_{DS} in a long channel device, because the gate exclusively controls the potential in the middle of the channel. The electrostatic potential $\phi(x,y)$ in the device of Figure 3.3 is only a function of y in the mid-channel region along $x = x'$. Thus the potential barrier that electrons surmount to reach the drain varies only with depth y. Whether current flow over this barrier is modelled by thermionic emission, diffusion, or thermionic emission-diffusion theory, the current density is exponentially dependent on the barrier height $\phi_b(y)$ [1]:

$$J(y) = J_0(y)\, e^{-q\phi_b(y)/kT} \qquad (3.6)$$

Figure 3.18 represents a calculated subthreshold potential distribution in the middle of a long-channel FET along the Figure 3.3 line $x = x'$ [1]. The exponential dependence of (3.6) suggests that the vast majority of current should flow at the depth of the potential minimum $y_{\phi min}$. As the gate is taken to an increasingly negative bias, the potential minimum increases to decrease I_{DS}, and $y_{\phi min}$ shifts slightly to a greater depth.

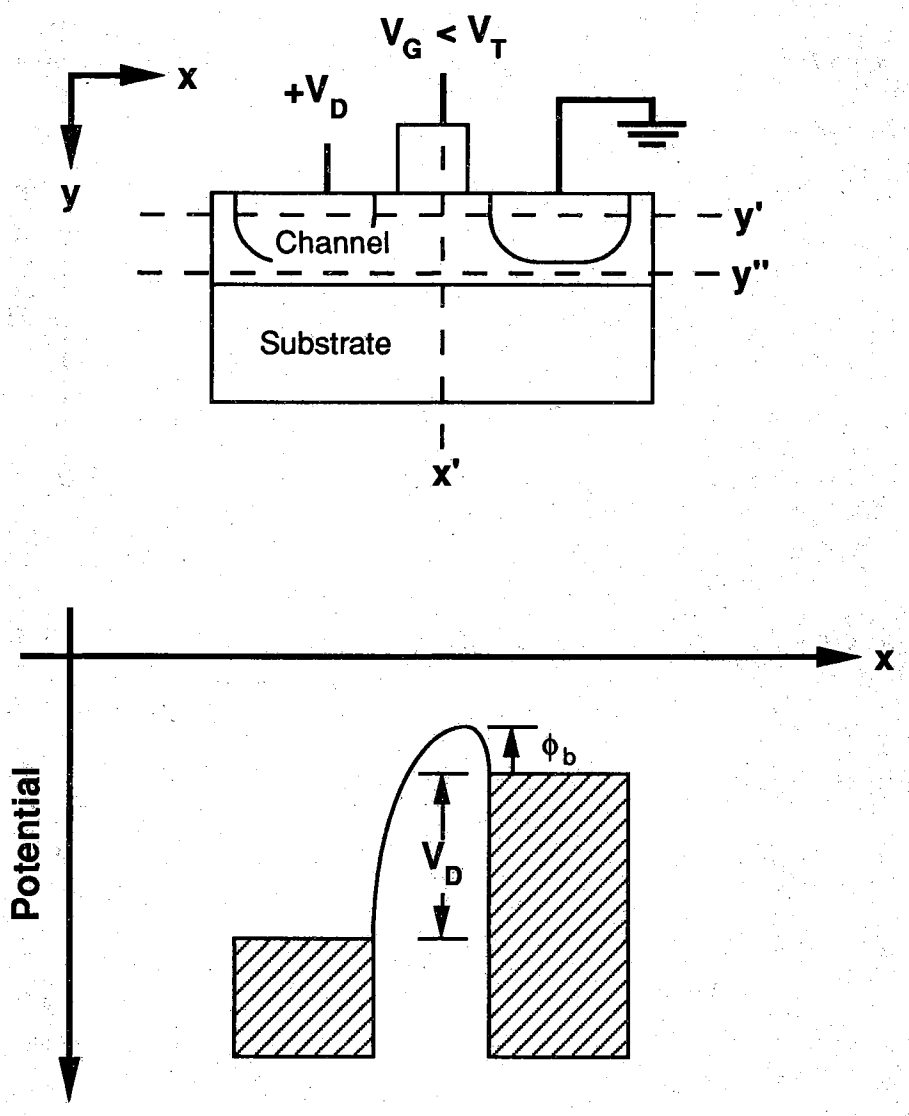


Figure 3.17 Short-channel source-to-drain subthreshold leakage. The barrier that source electrons must surmount to reach the drain is affected by the source/drain potentials, and the minimum potential path becomes a two-dimensional function of position.

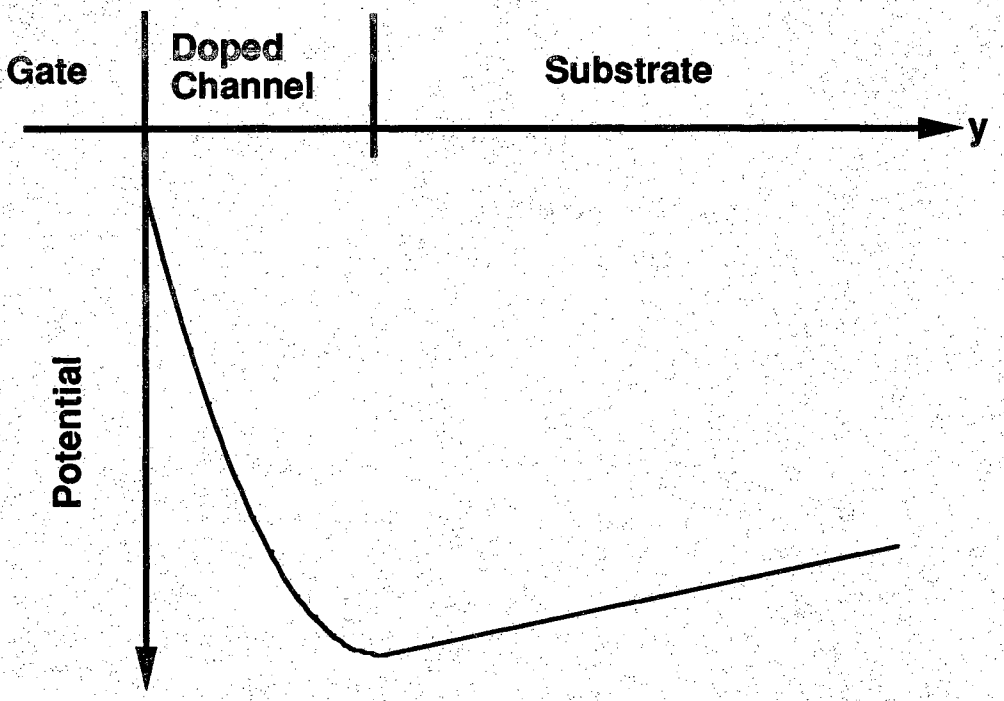


Figure 3.18 A potential diagram calculated along x = x' of Figure 3.3 for a turned-off long-channel FET.

In short-channel FET's, the electrical influence of the source and drain warrants a very complex 2-dimensional consideration of drain-to-source subthreshold leakage. There has been much work concerning the theoretical modelling and minimization of short-channel source-to-drain subthreshold leakage [1,31-40]. Only general results of these short-channel studies and their effect on FET subthreshold leakage current are discussed in this section.

As with the long-channel case, the analysis centers on the potential that carriers must surmount to reach the drain. The potentials throughout the device can be computed by solving Poisson's equation in two-dimensions. The near-gate channel regions (like (x',y') of Figure 3.17) are still largely controlled by the gate, but the source/drain bias significantly influences the potential deeper beneath the gate. Generally speaking this influence makes the sub-channel electric potential (e.g., ϕ(x',y'') of Figure 3.17) less sensitive to changes in the gate bias. Most subthreshold I_{DS} electrons will take the potential minimum path from source to drain.

Because the electrical influence of the gate on the minimum potential barrier is diminished in a short-channel FET, the rate at which I_{DS} drops with increasingly negative V_G also decreases. The change in I_{DS} with V_G remains exponential in nature, but the source-to-drain subthreshold ideality factor n_{Sub} is pushed farther above unity. This phenomena is observable for the experimental short-channel FET's of Section 3.3.3.

In extremely short-channel FET's ($L_{Gate} \sim 0.1$ μm), the source and drain potentials increasingly dominate the path I_{DS} carriers take. Beyond a certain V_G, the vast majority of leakage will occur in the deeper device regions whose potential is almost exclusively controlled by the source and drain. With minimal gate influence on the critical leakage path, I_{DS} becomes largely independent of V_G at larger gate biases. In this manner the I_{DMin} in extremely short-channel FET's is limited by drain-to-source leakage instead of drain-to-gate diode leakage [36].

3.3.3 Suppression of Short-Channel Effects Through Buried P-Layer

Since enhanced circuit speeds are largely driven by shrinking gate lengths, reducing detrimental short-channel effects in doped-channel GaAs FET's has been an important topic in recent years. In the early 1980's most GaAs MESFET and JFET processes simply placed an n-type channel layer on top of semi-insulating material. This insured the presence of large depleted areas under the device resulting in minimal parasitic substrate capacitances. However, transistors fabricated in this manner contained problems that seemed to preclude the fabrication of sub-micron gate length FET's satisfactory for use in LSI IC's.

Most of these problems were related to the interaction of device channel with the undoped substrate [37-40]. Changes to the electric potential of the undoped regions just beneath the channel affect the electrostatics of the doped FET channel, resulting in undesirable shifts of device current and threshold voltage. When this potential change is due to voltage applied to a nearby device, the problem is referred to as sidegating. When the sub-channel potential change is induced by the FET's own drain, the results are short-channel effects discussed in the previous section.

In 1985, Yamasaki et al. proposed the introduction of a lightly doped p-layer beneath the doped channel to reduce the magnitude and scope of these channel-to-substrate interactions [33]. Though the p-layer is entirely depleted by the heavier doping of the n-channel layer, the band bending it produces yields a potential barrier at the back of the channel (Figure 3.19). This potential barrier better confines subthreshold electrons, keeping them closer to the electrical influence of the gate. Additionally, the extent to which drain and sidegating fields reach into the middle of the channel is reduced by the higher donor concentration. Both these mechanisms relieve the dependence of channel characteristics on drain and adjacent device bias, resulting in a significant reduction of sidegating and short-channel effects. As one might expect from the above arguments, both buried p-layer doping and thickness effect the degree to which short channel effects are minimized [34-36,39,40].

The price that is paid for the buried p-layer is an increase in parasitic device-to-substrate capacitances which could cut operational

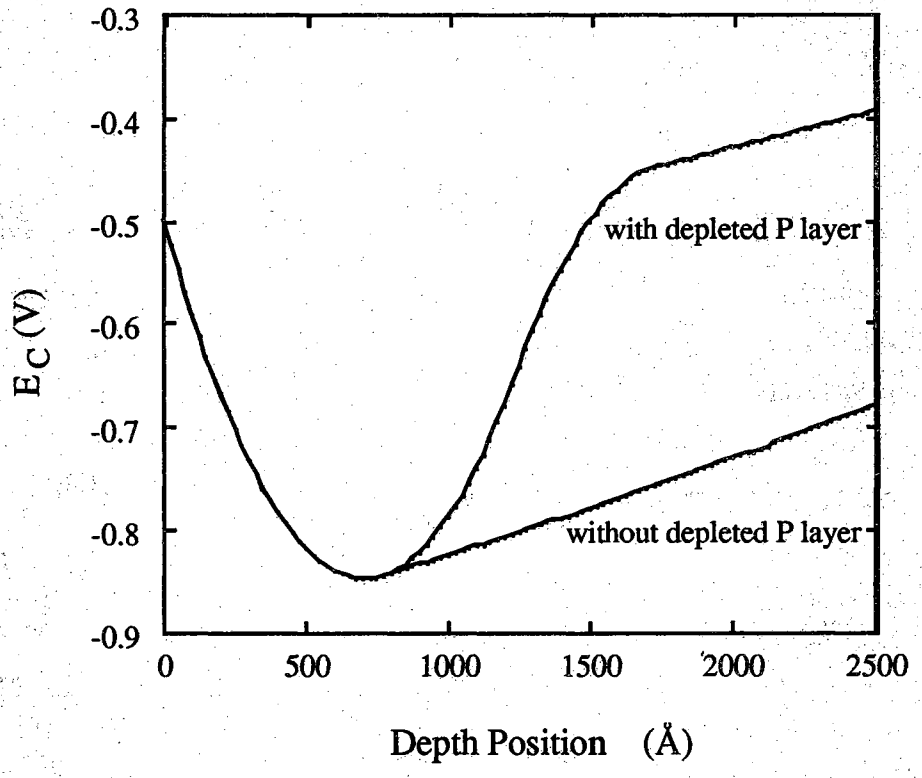


Figure 3.19 Conduction band cross-sections along the x = x' line of Figure 3.3 for FET's with and without buried p-layers. The doped-channel thickness has been adjusted so that the potential minimum occurs around 700 Å. After Reference [1].

circuit speed. Though depleted, the heavier p-doping charge beneath the device reduces substrate diode depletion depths resulting in increased device-to-substrate capacitances. There is also an increase in the FET body effect [53]. Many studies on MESFET integrated circuit performance as a function of buried p-layer doping profile were conducted in the late 1980's [34-36,39,40]. As one might expect from the arguments proposed above, short channel device characteristics improved as the buried p-layer charge (i.e., doping-thickness product) increased. The gains made in FET short channel performance appear to have outweighed the increase in parasitic device capacitance and body effect. Buried p-layers are standard to all GaAs doped-channel FET IC processes, and some use buried p-layers that are no longer entirely depleted [35,36].

3.3.4 Short-Channel I_{DS} Subthreshold Current Model

Although the device physics outlined in the previous section is complicated, the circuit level models for short-channel GaAs JFET and MESFET subthreshold drain-to-source leakage are not as complex. The I_{DS} subthreshold conduction is modelled quite well by [30]:

$$I_{DS} = I_{DSSub0}\left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right]\exp\left(\frac{q}{n_{Sub}\,kT}\left(V_{GS} - V_{T0} - \kappa V_{DS}\right)\right) \tag{3.7}$$

This expression is like the long channel I_{DS} leakage expression given in (3.2), but with the short channel threshold shift of (3.5) added. Under subthreshold conditions, short channel effects manifest themselves through an increased n_{Sub} and the threshold voltage shift of (3.5).

The parameters κ and n_{Sub} are uniquely determined by the two-dimensional device profile, so their theoretical modelling requires a full 2-D Poisson simulation of the short-channel device structure in question. The theoretical 2-D modelling of the epitaxial FET structures of Figure 3.20 was carried out by Dungan in Reference [1], and the results are summarized in Figures 3.20 through 3.26. These simulations analyzed the

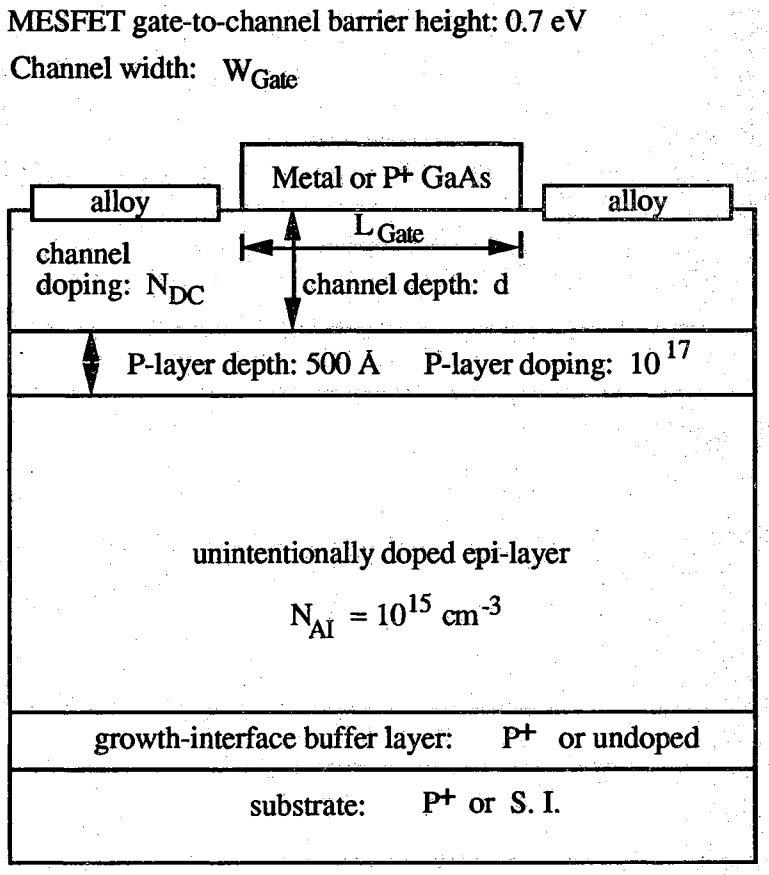


Figure 3.20 Generalized epitaxial FET structure simulated by Dungan. After Reference [1].

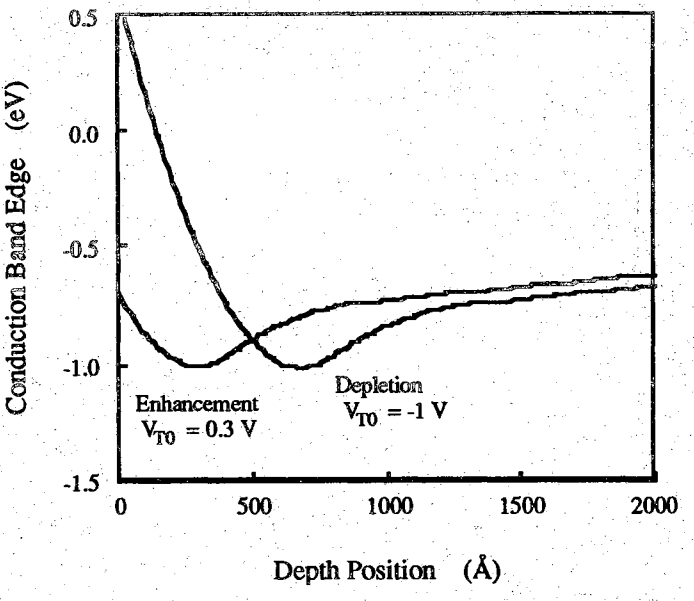


Figure 3.21 Simulated conduction band cross-sections through the gates of enhancement and depletion mode MESFET's. Channel doping is 5 x 10^{17} cm^{-3}, and $V_{GS} = V_{T0}$ - 0.1 V for both devices [1].

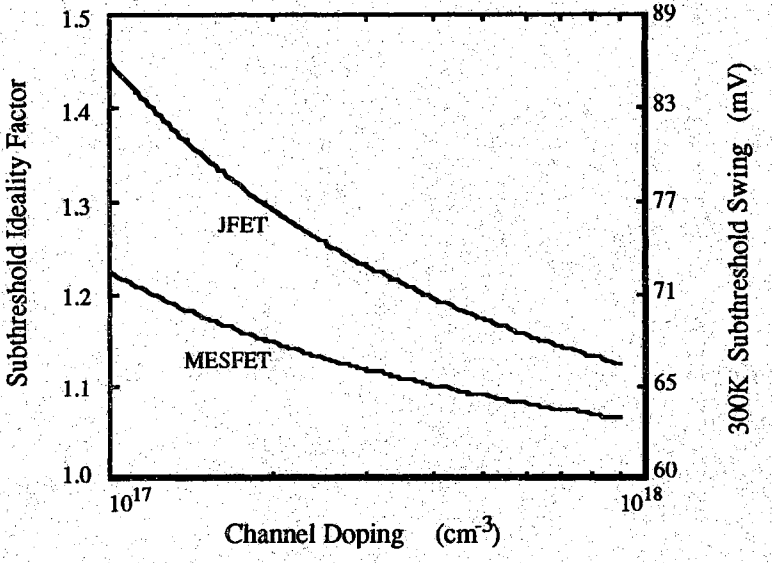


Figure 3.22 Simulated subthreshold ideality factor for a comparable JFET and MEFET. The channel depths are adjusted to make V_{T0} = 0.3 V in both devices, and L_{Gate} = 0.5 μm. After Ref. [1].

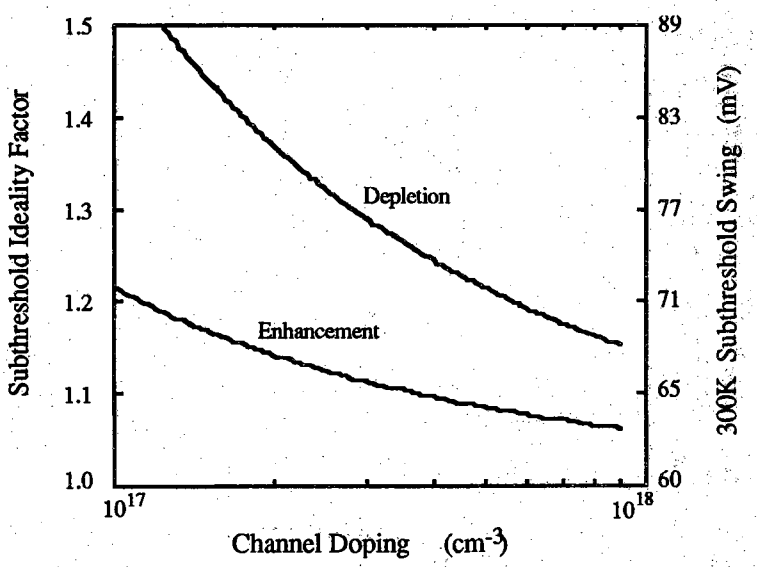


Figure 3.23 Simulated subthreshold ideality factor versus channel doping for enhancement and depletion mode MESFET's. Channel depths adjusted to maintain V_{T0} = 0.3 V and -1.0 V [1].

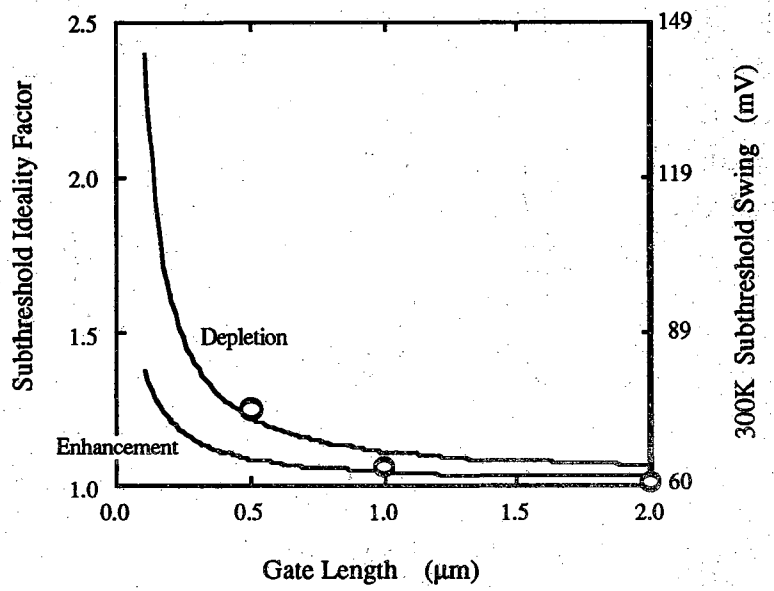


Figure 3.24 Subthreshold ideality factor versus gate length for enhancement and depletion mode MESFET's. Channel doping = 5 x 10^{17} cm^{-3}, and channel depths adjusted to maintain V_{T0} = 0.3 V. The circles represent subthreshold slopes measured on experimental E-MESFET's (see text). After Reference [1].

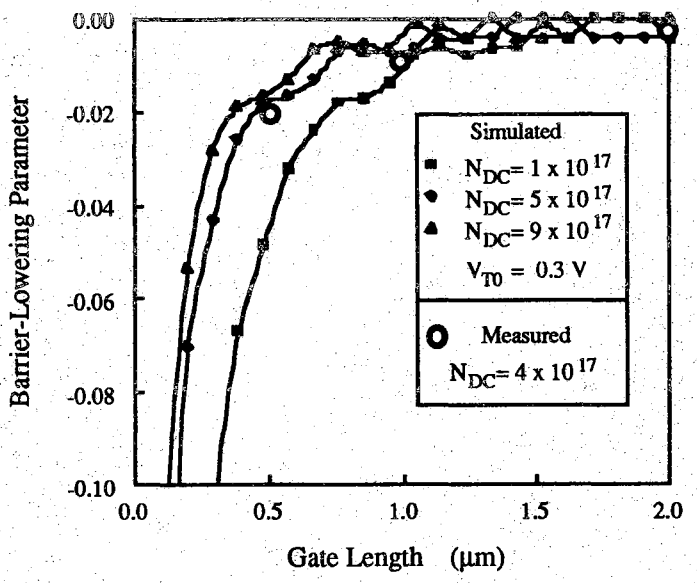


Figure 3.25 κ versus gate length for an enhancement-mode MESFET. Channel depth in simulations adjusted to maintain V_{T0} = 0.3 V. Circles represent κ's measured on experimental E-MESFET's (see text). After Reference [1].

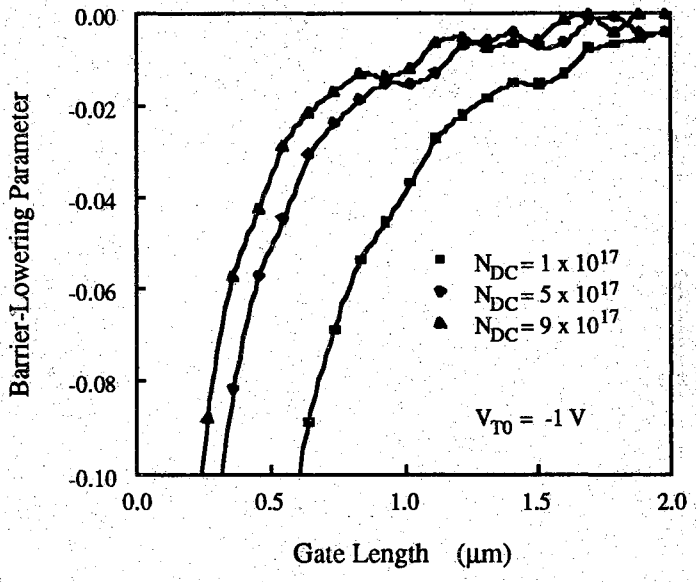


Figure 3.26 Simulated κ versus gate length for a depletion-mode MESFET. Channel depths adjusted to maintain V_{T0} = -1.0 V. After Ref. [1].

subthreshold behavior of enhancement-mode and depletion-mode MESFET's as functions of gate length and N-channel doping, and theoretical values for κ and n_{Sub} were calculated [1].

The main insights gained from these simulations are worth noting, because the general trends apply to ion-implanted FET's as well. As channel doping is increased (while compensating channel thickness to maintain the same V_{T0}), the devices become less susceptible to short channel effects. The potential minimum path is moved closer to the gate, so it is better influenced by changes in V_G. For the same reason, the simulated E-MESFET shows better subthreshold characteristics than the D-MESFET. The higher gate barrier of a JFET pushes the potential minimum deeper into the channel, so its subthreshold leakage characteristics are inferior to those of a MESFET with the same doping and V_{T0} (Figure 3.22).

3.3.5 Experimental Short-Channel Measurements

The epitaxial MESFET of Figure 3.5 has nearly has nearly the same structure as the $N_D = 5 \times 10^{17}$ cm^{-3} $V_{T0} = 0.3$ V E-MESFET simulated by Dungan [1]. Figures 3.27, through 3.29 show the measured leakage characteristics of experimental short channel devices fabricated using direct-write electron-beam lithography. The short-channel effects mentioned above are readily visible as the gate length is shrunk from 2 μm to 0.5 μm. The I_{DS} curve-shift associated with the drain bias steps (e.g., κ in (3.7)) grows as L_{Gate} decreases, and n_{Sub} follows a similar trend. Numerical values for κ and V_{T0} were extracted from the measured I_{DS} data using the procedure outlined in Reference [30]. When plotted against the theoretical data of Figures 3.24 and 3.25, the parameters extracted from the measured data are in good agreement with the Dungan's 2-D simulations.

Structural and doping profile differences cause the short-channel parameters to take on somewhat different values in ion-implanted FET's, but the general trends are the same. Table 3.1 compares the short-channel

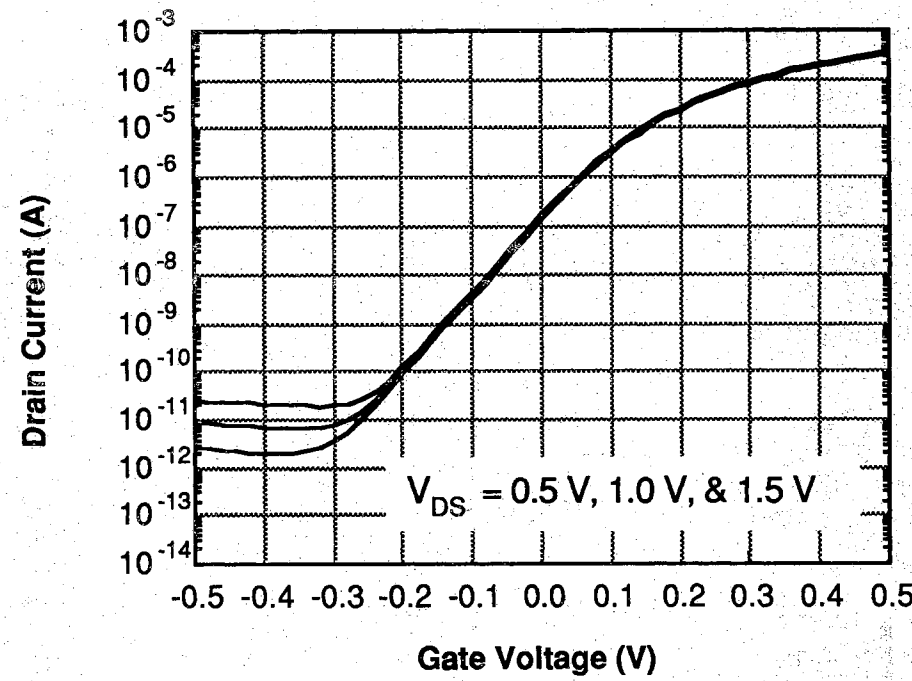


Figure 3.27 Experimental 2 x 30 μm^2 epitaxial MESFET subthreshold characteristics. $V_{T0} = 0.11$ V, $\kappa < 0.006$, $n_{Sub} = 1.01$.

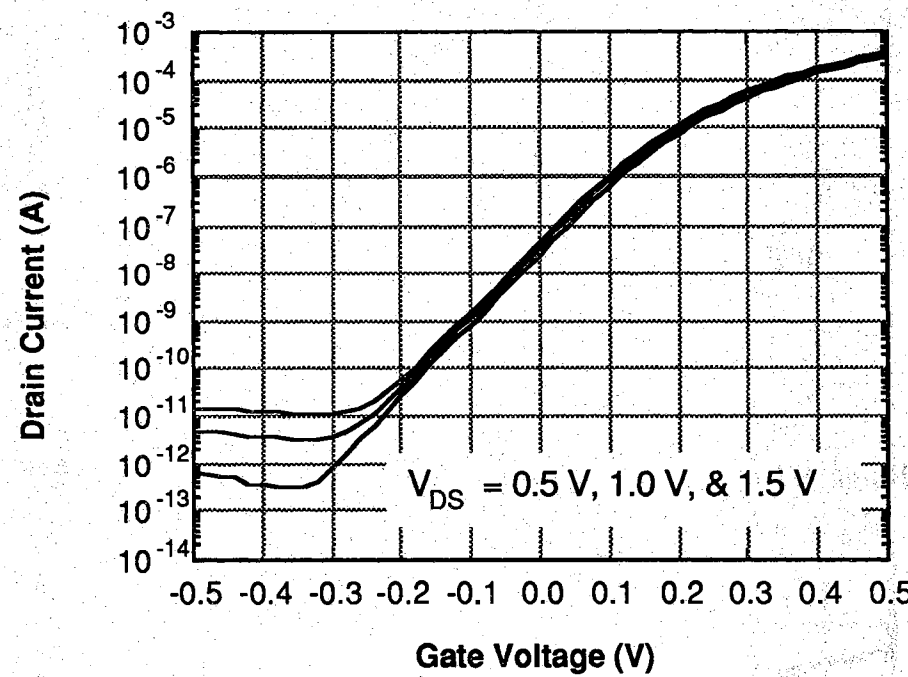


Figure 3.28 Experimental 1 x 30 μm^2 epitaxial MESFET subthreshold characteristics. $V_{T0} = 0.20$ V, $\kappa = 0.011$, and $n_{Sub} = 1.07$.

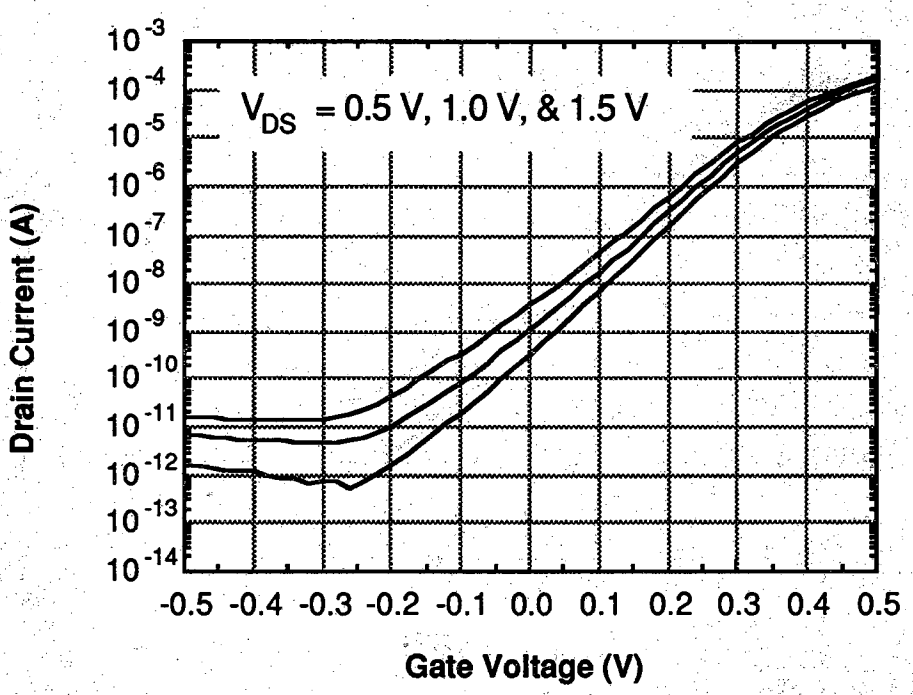


Figure 3.29 Experimental 0.5 x 30 μm^2 epitaxial MESFET subthreshold characteristics. V_{T0} = 0.33 V, κ = 0.022, and n_{Sub} = 1.26.

Table 3.1 Drain-to-source subthreshold short-channel parameters for selected MESFET's.

Device	L_{Gate} (μm)	V_{T0} (V)	κ	n_{Sub}
Purdue Epi-MESFET (Fig. 3.28)	1.0	0.20	-0.0109	1.11
Purdue Epi-MESFET (Fig. 3.29)	0.5	0.33	-0.0219	1.27
IBM Epitaxial MESFET [41]	0.5	0.29	-	1.25
Honeywell SAG MESFET [30]	1.0	0.10	-0.035	1.3
Honeywell SAG MESFET [34]	0.5	0.10	-	1.6
NTT SAINT MESFET [36]	0.1	-0.5	-	1.7
Texas Instruments D-MESFET [29]	1.0	-0.73	-0.0359	1.35

I_{SD} leakage parameters reported in published literature to the epitaxial MESFET results reported above.

Epitaxial short-channel JFET's were also characterized. These devices had the same structure of Figure 3.4, except the channel doping was reduced below 3 x 10^{17} cm^{-3} to give a V_{T0} of -0.25 V. Measured subthreshold slopes as a function of gate length are plotted in Figure 3.30. Down to L_{Gate} = 0.5 μm these JFET's exhibited satisfactory drain-to-source turn-off characteristics, as I_{DMin} was determined by gate-to-drain or drain-to-substrate diode leakage (Section 3.2) and n_{Sub} stayed less than 1.5. Through careful E-beam assisted lithography, a 0.25 μm-drawn gate length JFET was obtained, but it's leakage characteristics were not satisfactory (Figure 3.31). There are monsterous increases in κ and n_{Sub} which push the drain current minimum beyond reasonable logic GaAs logic biases. I_{DS} never becomes insignificant compared to diode leakages, which implies that source-to-drain conduction through the substrate is dominant. The physical gate length of this transistor is most likely less than 0.25 μm due to etchant undercutting associated with the P^+ cap removal etch (Figure 5.3, Step 4).

3.4 Power Dissipation

The importance of standby power dissipation is underscored by the fact that the average RAM cell spends 99% of its time in the idle unaddressed state. The idle-state power consumption of a DRAM cell is dictated by the leakages of the turned-off access transistor through the current-voltage product. As they pertain to the storage time of the device through I_D, most of the off-state leakages present have already been mentioned in Sections 3.2 and 3.3.

3.4.1 Substrate-to-Gate Punchthrough Current

A major source of transistor leakage current was overlooked in Sections 3.2 and 3.3 due to the fact that it is not related to I_D. A depletion-

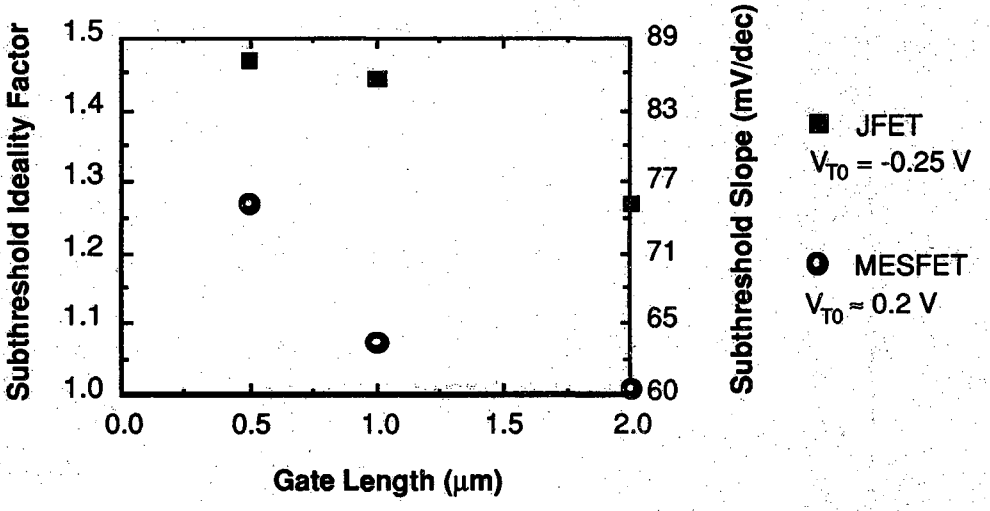


Figure 3.30 Experimentally measured epitaxial JFET and MESFET subthreshold slopes.

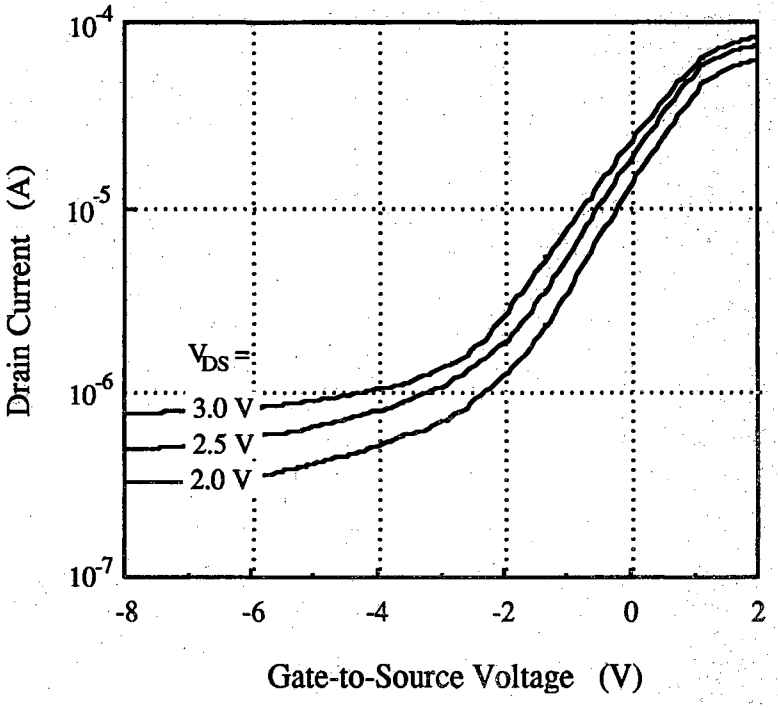


Figure 3.31 Measured very short channel epitaxial JFET subthreshold characteristics. $L_{Gate} \sim 0.25$ μm, $W_{Gate} = 20$ μm.

mode FET is turned-off by applying a negative V_G so that the N channel becomes entirely depleted. With the gate and substrate channel depletion regions touching each other a puncthrough conditon occurs [119,131]. The potential barrier between the gate and the substrate is reduced to the point where a substantial number of substrate holes flow to the negatively-biased gate (Figure 3.32). Although high resistivity substrates can limit the current flow somewhat, punchthrough currents can greatly influence the static DRAM cell power dissipation. Figure 3.33 shows the leakage currents that flow in a JFET transistor biased at its drain current minimum. The vast majority of off-state power dissipation arises from gate-to-substrate punchthrough. The punchthrough current in this particular device is terribly exacerbated by the fact that only 1 μm of insulating material isolates it from a P^+ substrate, and the effective punchthrough area includes a 20 x 20 μm^2 gate probe contact (Figure 3.13b). Even so, the 0.15 μW off-state power dissipation compares very favorably with the 1 to 10 μW found in GaAs SRAM cells.

Punchthrough current often plays a major role in DRAM cell power dissipation, but it is not always dominant. Figure 3.34 shows the gate and drain currents of two 10 x 350 μm^2 ring-gate MESFET's, one with an $(NH_4)_2S$-treated gate and the other with a convential untreated gate. The large gate-to-drain leakage of the conventional MESFET swamps out the punchthrough current, making I_{DG} the dominant power consuming leakage. Even so, the off power consumption of this large device is less than 10 nW. In the $(NH_4)_2S$-treated sample with reduced gate-to-drain diode leakage, the punchthrough current is readily visible as it becomes the largest device current for $V_G < -0.4$ V. A reasonable storage-state bias point for this device is $V_G = 0.5$ V, and although punchthrough is significant, the power consumption is less than 1 nW. In a non-ring-gate MESFET the parasitic gate overlay diode could become a primary source of transistor off-current (Figure 3.15). However the gate current measured in Figure 3.16 shows that this is not a particularly serious problem on an insulating substrate, as the large 20 x 20 μm^2 off-mesa gate contact draws less than 20 nW.

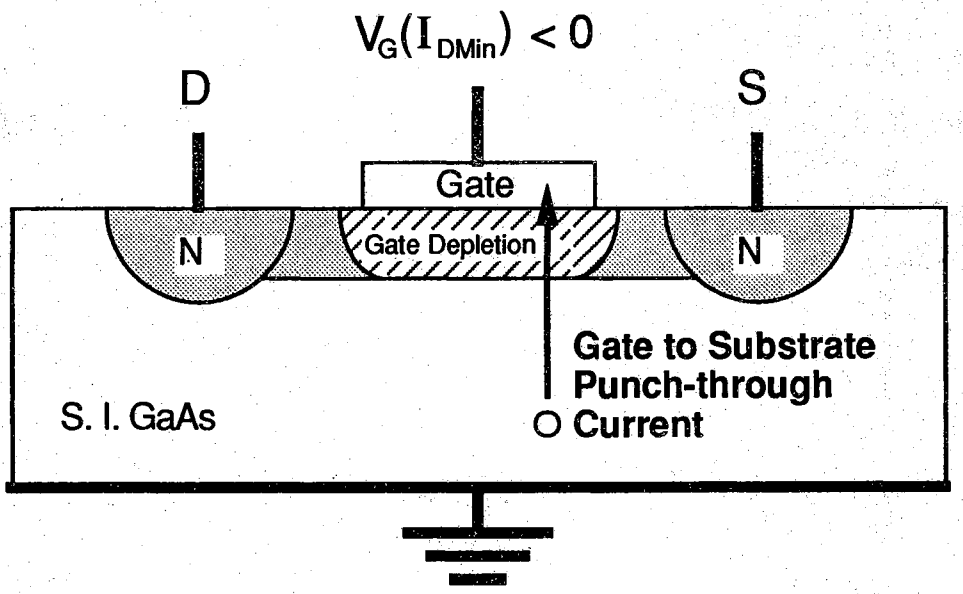


Figure 3.32 Substrate-to-gate hole punchthrough current in a doped-channel GaAs FET. When sufficiently negative voltage is needed to turn off the access transitor, the punchtrough current can be the largest source of DRAM storage-state power.

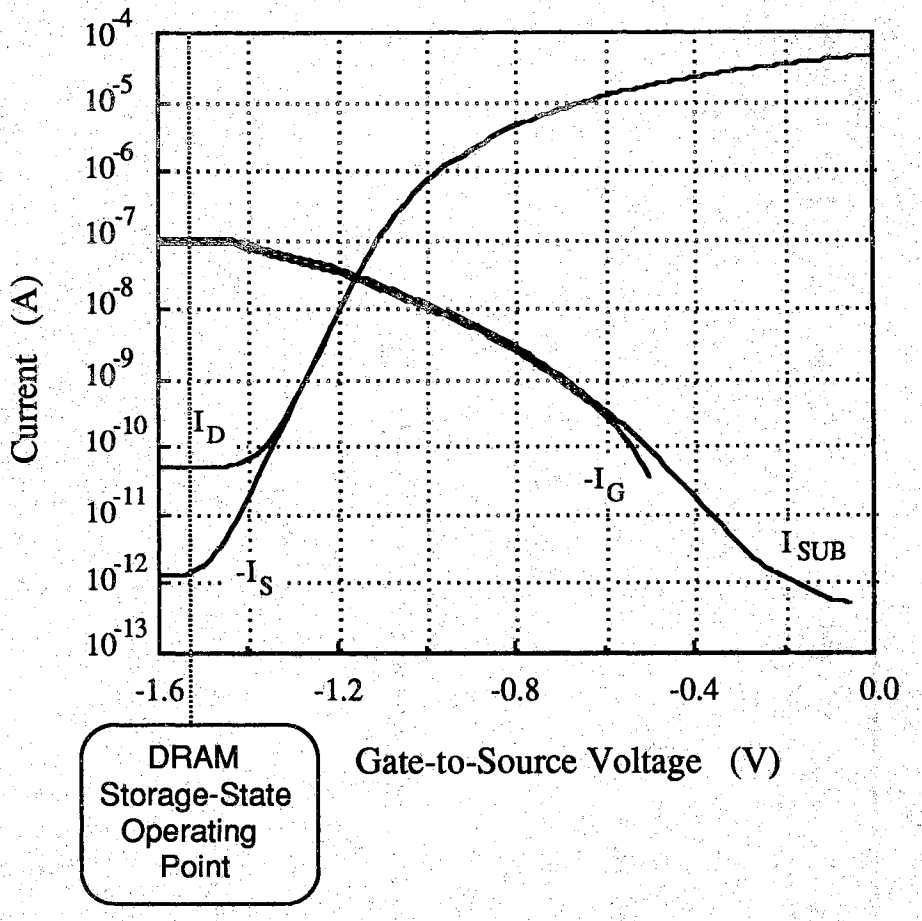


Figure 3.33 Measured currents in a 2 x 20 μm^2 JFET as a function of gate voltage. The source and substrate are grounded, and V_{DS} = 0.5 V. The large I_G and I_{Sub} is due to gate-to-substrate punchthrough exacerbated by a non-insulating substrate (see text).

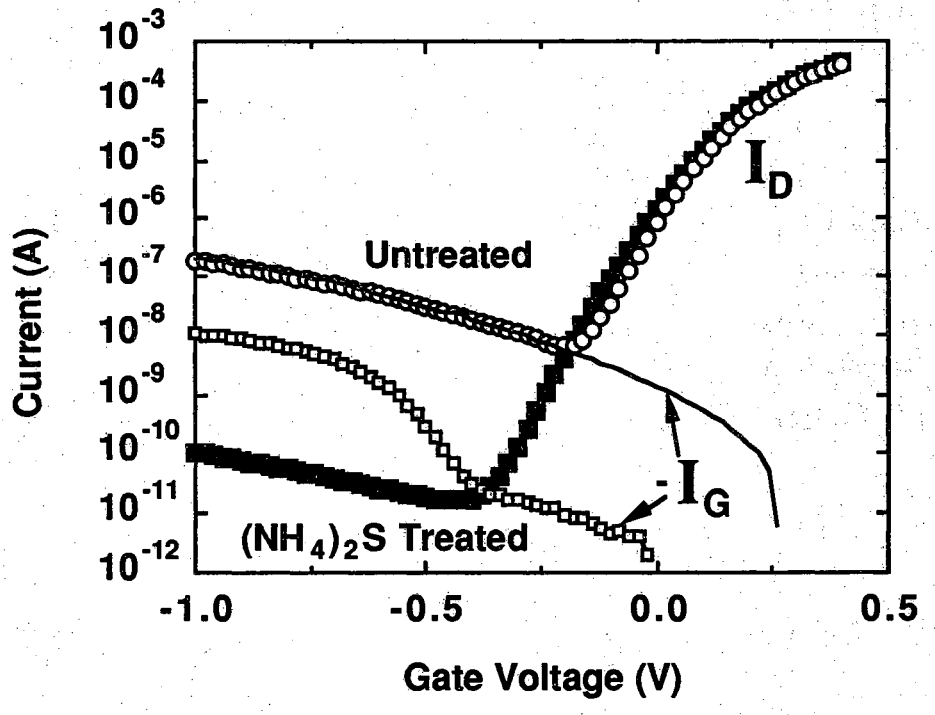


Figure 3.34 Drain and gate currents in 10 x 350 μm^2 $(NH_4)_2S$-treated and untreated MESFET's. Source and substrate grounded, V_{DS} = 0.5. The gate to substrate punchthrough current is insignificant compared to I_{DG} in the unctreated device, but it is readily visible below $V_G < 0.5$ V in the $(NH_4)_2S$-treated MESFET.

3.4.2 Source Biasing

In addition to power consumption, gate punchthrough is undesirable because it could lead to unwanted substrate noise and sidegating problems. To eliminate off-state gate-to-substrate current flow, one can use enhancement-mode access so that I_{DMin} occurs at $V_G = V_{Subs} = 0$. One way to accomplish this is to simply use an enhancement mode access transistor with the proper positive threshold voltage. Under this scheme one would apply positive voltages to read and write the cell, but some care in the selection of operating voltages must be taken to prevent excessive forward-biased gate currents.

A depletion-mode N-channel FET with $V_{T0} < 0$ can also be biased so that it is turned off at $V_G = V_{Subs} = 0$. Instead of turning-off the channel by applying a negative voltage to the gate, one can equivalently take the source and drain positive with respect to the gate and substrate. As opposed to using V_G to raise the channel barrier in Figure 3.3, the source Fermi level can be pushed down with positive source bias V_{SB} to enlarge ϕ_b. This enables a depletion-mode device to function effectively as a pseudo-enhancement-mode access transistor, whereby only positive voltages are employed to control the on/off state of the device.

Naturally, source biasing changes the operational device parameters somewhat through the body effect [53]. The channel-to-substrate depletion widths will be increased by the additional reverse bias, but most of this change is absorbed by the lightly-doped substrate instead of the conducting channel. This fact combined with the low operating voltages used in digital GaAs IC's make the body effect manageably small for the source biases of interest ($V_{SB} < 2$ V). Given a constant source bias V_{SB}, the change in FET characteristics is effectively modelled by shifting the threshold voltage. The epitaxial JFET's of Figure 3.4, which showed $V_{T0} = -1.0$ V at $V_{SB} = 0$, exhibited a $V_T = -0.87$ V at $V_{SB} = 1.0$ V. The increased drain-to-substrate bias causes some additional drain-to-substrate leakage current to flow (Section 3.2.5).

3.5 Access Transistor Operating Voltage Requirements

The access transistor of a dynamic memory cell must be capable of supplying a very large range of drain-to-source currents. To achieve high-speed operation the capacitor-to-bitline current must be as large as possible during reading and writing, while in the storage state the drain current must be extremely small to maintain the charge on the capacitor between refresh cycles. The choice of proper device threshold voltages and operating voltages is critical if these access transistor design goals are to met with GaAs JFET and MESFET technologies.

3.5.1 Key Device Characteristics

There are three key FET characteristics which will govern the range of voltages employed in the DRAM cell. Figure 3.35 illustrates these physical parameters on an I_G versus V_{GS} characteristic, and they are individually discussed and estimated in the following sub-sections.

3.5.1.1 Forward-Biased Gate Leakage

Without the gate insulator of the MOSFET access transistors used in silicon DRAM cells, the range of gate biases which can be applied to the gate of a GaAs JFET or MESFET is restricted. If too much positive voltage is placed on the gate to turn on the access transistor, the forward-biased gate diode will draw as much current as the turned-on transistor channel. This would clearly interfere with DRAM cell read operations, as a lot of the charge that's supposed to be sensed on the bitline will instead be lost to the wordline when the access FET is turned on.

V_{GM} is defined as the maximum forward bias which can be applied to the gate-to-channel diode before unacceptably large currents begin to flow. Although somewhat arbitrary, a reasonable definition of unacceptably large in this work lies at a 1:10 ratio of gate diode current to channel current. Technically speaking, the gate voltage at which this ratio

occurs will change with lateral device dimensions, threshold voltage, and gate diode quality. However the similar geometries and small thresholds of most GaAs FET's dictate that V_{GM} is primarily established by access transistor type through the magnitude of the gate current. Typical values taken from published literature and measurements on the epitaxial FET structures of Figure 3.4 and 3.5 place $V_{GM} \cong 0.6$ V for conventional Schottky gate MESFET's and $V_{GM} \cong 1.3$ V for PN junction gate JFET's [43]. The reduction in forward-biased gate current in $(NH_4)_2S$-treated Au gate MESFET's suggest that they have a $V_{GM} \cong 0.8$ V [15-18].

3.5.1.2 Turn-On Gate Voltage

To obtain high speed operation one should maximize the access transistor on current. It is useful in the ensuing discussions to define ΔV_{on} as the voltage beyond threshold which must be applied to the gate to achieve the desired bitline-to-capacitor current during reading and writing. This number is unique to each FET, so it should be selected from the access transistor's I_{DS} versus V_{GS} characteristics. To prevent positive V_G from causing excess gate current, ΔV_{on} should satisfy:

$$V_T + \Delta V_{on} < V_{GM} \tag{3.8}$$

which can be re-written as:

$$\Delta V_{on} < V_{GM} - V_T \tag{3.9}$$

To get a decent amount of current out of a typical GaAs FET, ΔV_{on} should be at least 0.5 V. The write speed will be maximized by employing as large a ΔV_{on} as (3.9) will allow; however, the considerations discussed in Section 3.5.2 show that too large a ΔV_{on} will cut into the available logic swing.

3.5.1.3 Turn-Off Gate Voltage

In the storage state one wants to minimize access transistor drain current, so the wordline off voltage $V_{WL(off)}$ should be near the drain current minimum of subthreshold leakage characteristic (Figure 3.1). However, as outlined in Sections 3.2 and 3.3, the location of the minimum $V_G(I_{DMin})$ is very device specific as it is a function of threshold voltage, subthreshold slope, and gate diode leakage. Noise considerations clearly dictate that $V_{WL(off)}$ should be more negative than $V_G(I_{DMin})$, due to the fact that the current changes much less with voltage in the I_{DG}-limited subthreshold regime than in the I_{DS}-subthreshold regime, (Figure 3.1). In the I_{DG}-limited regime the increase in gate current with decreasing V_G is typically smaller in JFET's than the MESFET's (Figure 3.7), so there may be a significant storage time versus noise margin design trade off in some MESFET's (e.g. the MESFET's of Figure 3.34).

In the discussion of access transistor operating voltages, it is convenient to define $\Delta V_{off} > 0$ as the amount of voltage below threshold that the wordline is taken to in the DRAM cell storage state:

$$\Delta V_{off} = V_T - V_{WL(off)} = V_T - V_G(I_{DMin}) + V_{NM} > 0 \qquad (3.10)$$

V_{NM} is the noise margin voltage to be added on beyond $V_G(I_{DMin})$ to insure the device is always biased in the I_{DG}-limited subthreshold regime. A reasonable neighborhood for V_{NM} is 0.1 to 0.2 V. Estimates for ΔV_{off} can be calculated from noise margin requirements and the subthreshold characteristics of the FET's being considered as DRAM access transistors. Room-temperature values of ΔV_{off} that would apply to various GaAs doped-channel FET's if they were operated as DRAM cell access transistors are tabulated in Table 3.2.

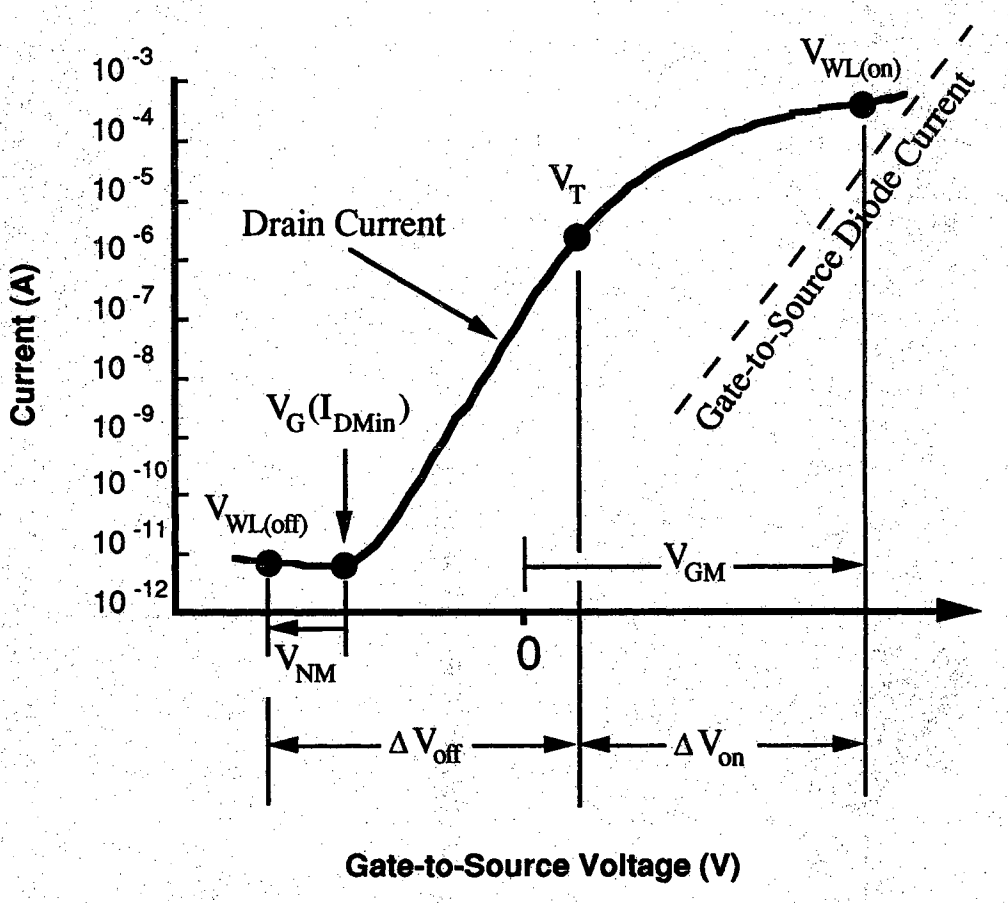


Figure 3.35 Graphical definition of GaAs FET physical parameters and operating voltages. From the FET I_D versus V_{GS} (solid line) and I_{GS} versus V_G (dashed line) characteristics, the device parameters V_T, ΔV_{off}, ΔV_{on}, and V_{GM} can be determined. These are in turn used to choose appropriate operating voltages $V_{WL(off)}$, $V_{WL(on)}$, V_{high}, and V_{low} as described in Sections 3.5.2 and 3.5.3. V_{GM} is taken to be the gate voltage at which 10 $I_{GS} = I_D$ (see text). Arbitrary FET characteristics are shown for illustration purposes only.

Table 3.2 Estimates of ΔV_{off} at room-temperature for selected GaAs FET's. The current minimums were determined from V_{DS} = 1.0 V or 0.5 V subthreshold characteristics.

Device	L_{Gate} (μm)	V_{T0} (V)	n_{Sub}	$\Delta V_{off} - V_{NM}$ (V)
Unt. RG MESFET (Fig. 3.8)	10	0.05	1.2	0.25
$(NH_4)_2S$ RG MESFET (Fig. 3.8)	10	0.05	1.2	0.45
Purdue Epi-MESFET (Fig. 3.28)	1.0	0.20	1.11	0.53
Purdue Epi-MESFET (Fig. 3.29)	0.5	0.33	1.27	0.6
Honeywell SAG MESFET [30]	1.0	0.10	1.3	0.29
Honeywell SAG MESFET [34]	0.5	0.10	1.6	0.4
NTT SAINT MESFET [36]	0.1	-0.5	1.7	0.4
Texas Instruments D-MESFET [29]	1.0	-0.73	1.35	0.37
Purdue RG Epi-JFET (Fig. 3.12)	5	-1.0	1.25	0.4

3.5.2 Fundamental Operating Voltage Requirements

To function adequately, but not necessarily optimally, all the access transistor must do is provide lots of on current and little off current. By choosing the proper operating voltages both JFET's and MESFET's can meet these requirements. This section examines the voltages used to operate functional GaAs DRAM cells.

To maximize the amount of charge stored in the cell the difference between the logic low voltage V_{low} and the logic high voltage and V_{high} should be as large as possible. Maintaining a reverse bias on the channel-to-substrate diode restricts V_{low} to positive voltages:

$$V_{low} \geq 0 \tag{3.11}$$

V_{high} is limited by the positive voltage that can be placed on the gate of the access transistor. To conduct a significant amount of current in the turned-

on state, V_G should be biased as much above threshold as V_{GM} will allow before excessive gate currents are drawn (Section 3.5.1.1). Therefore:

$$V_{WL(on)} < V_{low} + V_{GM} \tag{3.12}$$

To insure that all of V_{high} gets written to the storage capacitor, the gate of the access transistor should be held a threshold voltage drop above V_{high} [42,43]:

$$V_{WL(on)} > V_{high} + V_T \tag{3.13}$$

Relation (3.13) is a sufficient condition for writing the DRAM cell, but it does not assure that the writing of V_{high} will take place with the desired speed. To meet access transistor speed requirements when writing a V_{high}, V_{GS} must be held ΔV_{on} above (3.13):

$$V_{WL(on)} \geq V_{high} + V_T + \Delta V_{on} \tag{3.14}$$

The combination of (3.12) and (3.14) defines the range for $V_{WL(on)}$:

$$V_{high} + V_T + \Delta V_{on} \leq V_{WL(on)} < V_{low} + V_{GM} \tag{3.15}$$

Relation (3.15) places a restriction on V_{high}:

$$V_{high} \leq V_{low} + V_{GM} - V_T - \Delta V_{on} \tag{3.16}$$

The gate of the access transistor should never be forward-biased in the off state. Thus:

$$V_{WL(off)} \leq V_{low} \tag{3.17}$$

For sufficient access transistor turn-off in the storage state, V_{GS} should always be less than $V_T - \Delta V_{off}$. Therefore:

$$V_{WL(off)} - V_{low} \leq V_T - \Delta V_{off} \quad (3.18)$$

Which leads to:

$$V_{WL(off)} \leq V_T - \Delta V_{off} + V_{low} \quad (3.19)$$

The union of (3.17) and (3.19) defines the acceptable range of $V_{WL(off)}$.

Given a GaAs FET with physical parameters V_T, V_{GM}, ΔV_{on}, and ΔV_{off}, the above relations specify the range of DRAM cell operating voltages. This range of voltages is considered non-optimal because it does not attempt to set $V_{WL(off)} = 0$ V to minimize standby-state gate currents (Section 3.4). However the experimental results of Chapters 4 and 5 clearly show that test DRAM cells can operate under these conditions.

To maximize logic swing, (3.11) and (3.16) should be treated as equalities, and this will uniquely specify $V_{WL(on)}$ (= V_{GM}) through (3.15) and the maximum value of $V_{WL(off)}$ through (3.19). The resulting GaAs DRAM cell operating voltages are plotted as a function of access transistor threshold voltage V_T in Figures 3.36 and 3.37. These plots are based on reasonable estimates for the device physical parameters V_{GM}, ΔV_{on} and ΔV_{off}. The disparity between the operating voltages of the JFET and the MESFET arises from the difference in V_{GM}. The logic swing of both FET's increases with more negative device threshold, but this benefit must be weighed against increased leakage from larger drain-to-source biases on the access transistor and the larger voltage swing required to drive the wordline between $V_{WL(on)}$ and $V_{WL(off)}$. Although it is not apparent from the operating voltage plots, it is important to note that one can sacrifice some logic swing to allow a larger ΔV_{on} to increase the transistor read/write current. Similarly, given a specified logic swing, shifting the threshold negative also allows larger values of ΔV_{on}. Although not shown, it should be noted that the improved V_{GM} of an $(NH_4)_2S$-treated MESFET would allow for larger logic swings than the conventional MESFET of Figure 3.37.

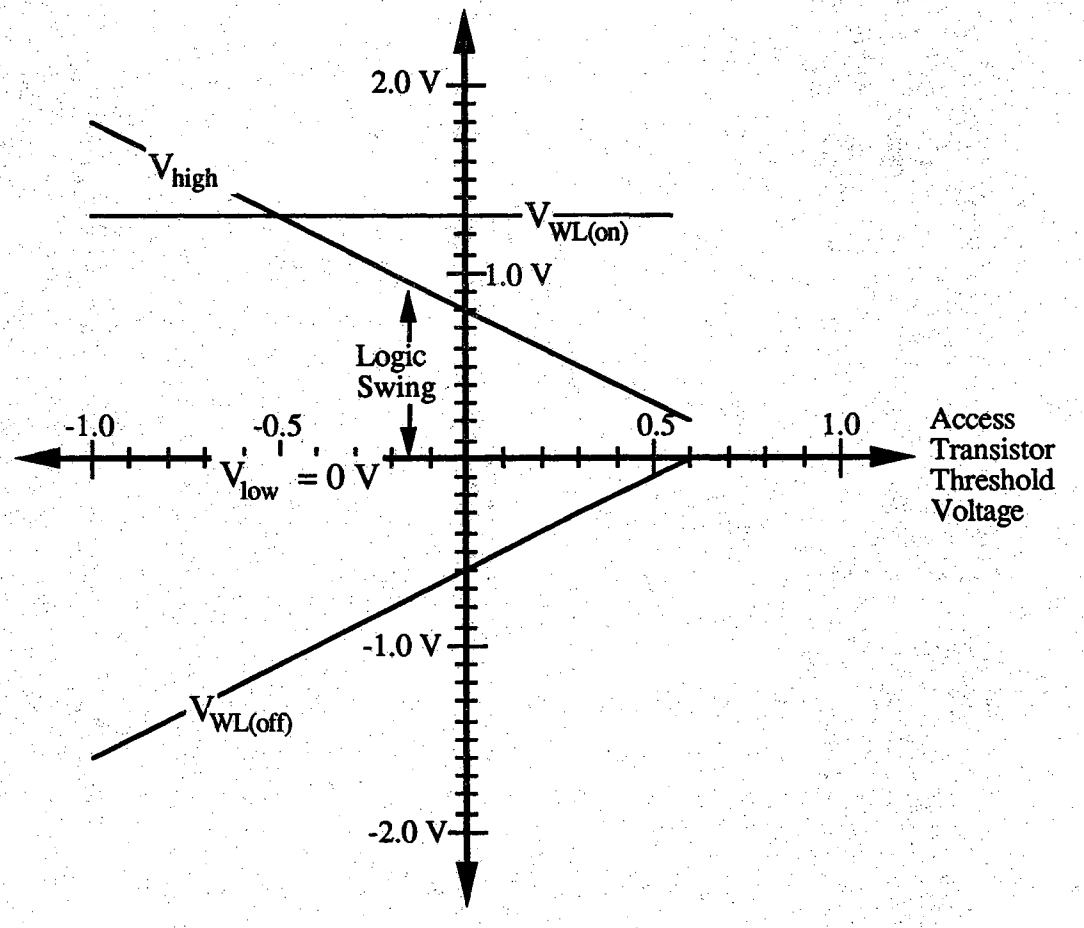


Figure 3.36 Generalized JFET DRAM cell operating voltages as a function of access transistor threshold voltage. The voltages shown maximize logic swing (see text). Generalized JFET parameters used to generate plot: V_{GM} = 1.3 V, ΔV_{on} = 0.5 V, ΔV_{off} = 0.6 V (Section 3.5.1).

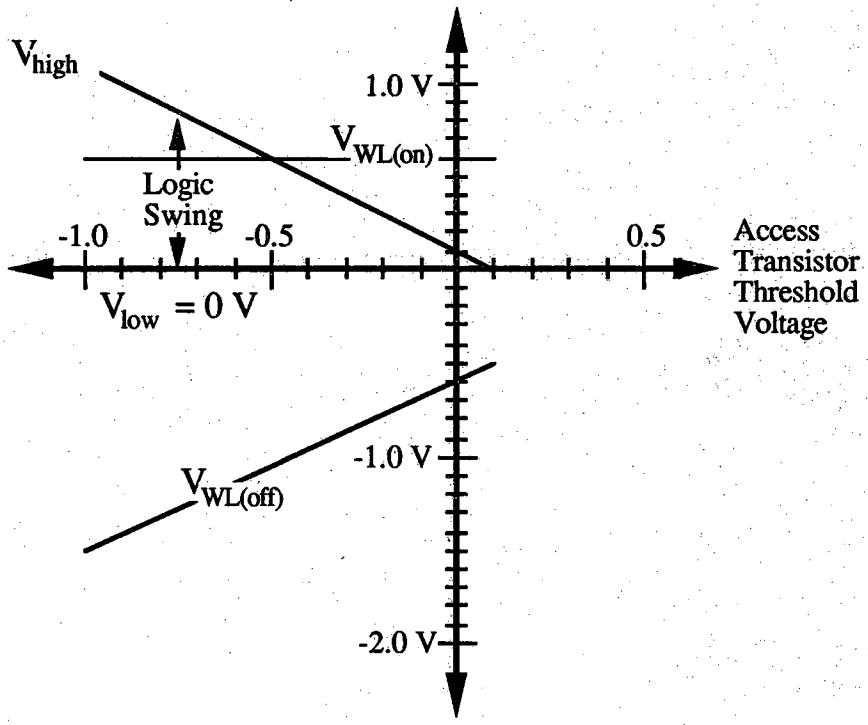


Figure 3.37 Generalized MESFET DRAM cell operating voltages as a function of access transistor threshold voltage. The voltages shown maximize logic swing (see text). Generalized MESFET parameters used to generate plot: V_{GM} = 0.6 V, ΔV_{on} = 0.5 V, ΔV_{off} = 0.6 V (Section 3.5.1).

3.5.3 Pseudo-Enhancement Access Operating Voltages

As introduced in Section 3.4, it would be highly advantageous to have the storage state wordline voltage $V_{WL(off)}$ equal to zero volts. This would eliminate parasitic substrate-to-gate currents that could result in sidegating noise and greatly increased power dissipation. By shifting V_{low} to a positive voltage, the source-biasing technique of Section 3.4.2 can be applied to set:

$$V_{WL(off)} = V_G = V_{Subs} = 0 \tag{3.20}$$

This psuedo-enhancement-mode access scheme eliminates off-state substrate-to-gate current. When (3.20) is substituted into (3.19), the result is an additional restriction on V_{low}:

$$V_{low} \geq \begin{Bmatrix} \Delta V_{off} - V_T \\ 0 \end{Bmatrix} \tag{3.21}$$

Given a GaAs FET with physical parameters V_T, V_{GM}, ΔV_{on}, and ΔV_{off}, relations (3.20), (3.21), (3.16), (3.15), (3.17), and (3.19) (which are most easily considered in that order) specify the DRAM operating voltages that allow the elimination of off-state substrate-to-gate current. Treating relations (3.21) and (3.16) as equalities yields the largest available logic swing, and similar to the previous section one can plot the operating voltages as a function of access transistor threshold voltage (Figures 3.38 and 3.39). Technically speaking the source bias induced by $V_{low} > 0$ will cause a body effect shift in device characteristics (Section 3.4.2). However this can be compensated for in device design by selecting V_{T0} so that $V_T(V_{SB} = V_{low})$ becomes the desired threshold.

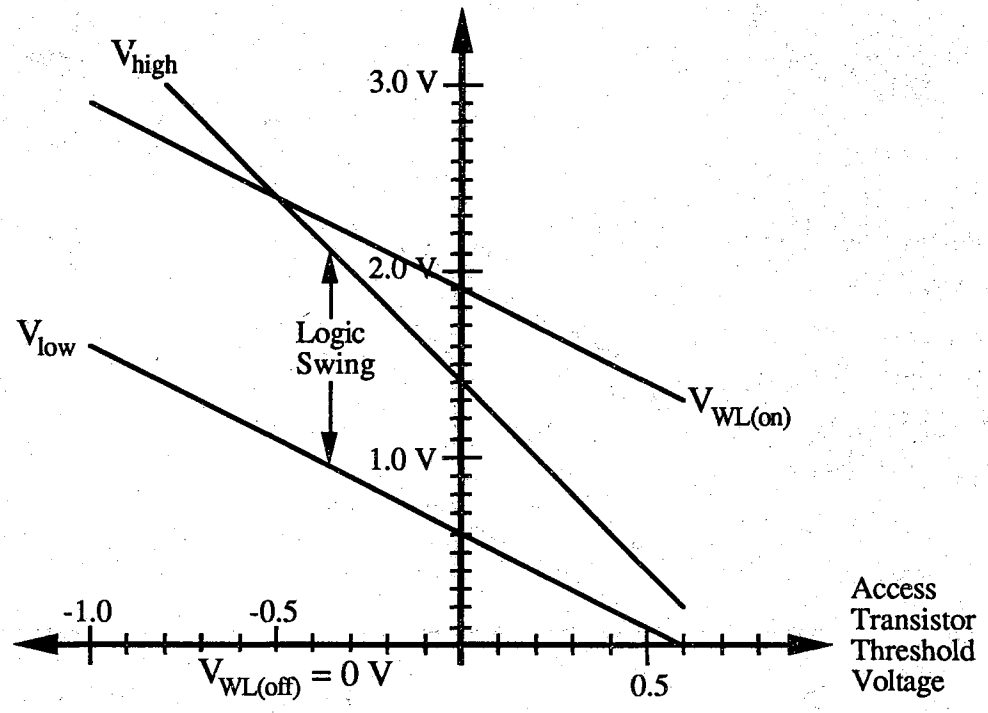


Figure 3.38 Generalized JFET DRAM cell operating voltages under the pseudo-enhancement-mode access scheme as a function of access transistor threshold voltage. The voltages shown maximize logic swing while minimizing storage state power dissipation by setting $V_{WL(off)} = 0$ V (see text). Generalized JFET parameters used to generate plot: $V_{GM} = 1.3$ V, $\Delta V_{on} = 0.5$ V, $\Delta V_{off} = 0.6$ V (Section 3.5.1).

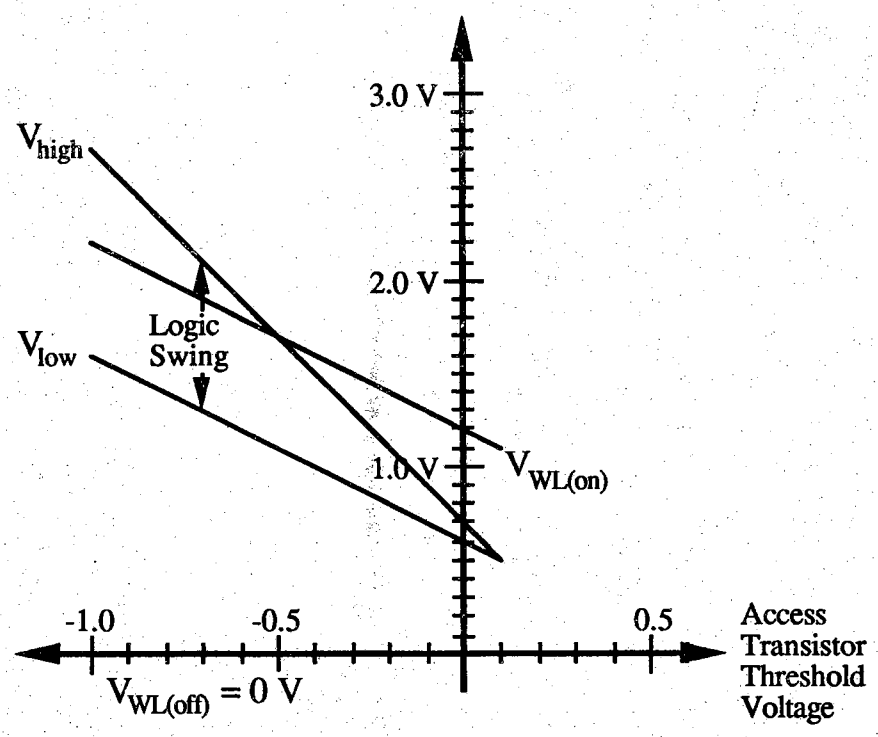


Figure 3.38 Generalized MESFET DRAM cell operating voltages under the psuedo-enhancement-mode access scheme as a function of access transistor threshold voltage. The voltages shown maximize logic swing while minimizing storage state power dissipation by setting $V_{WL(off)} = 0$ V (see text). Generalized MESFET parameters used to generate plot: $V_{GM} = 0.6$ V, $\Delta V_{on} = 0.5$ V, $\Delta V_{off} = 0.6$ V (Section 3.5.1).

CHAPTER 4 - GaAs DRAM CELLS

4.0 Introduction

This chapter combines the storage capacitor and access transistor concepts presented in Chapters 2 and 3 into complete operational DRAM cells. Sections 4.1 and 4.2 cover the fabrication, characterization, and successful room-temperature operation of JFET- and MESFET-accessed DRAM cells. The cells were based on the experimental epitaxial PN junction capacitors and FET's presented previously, so their behavior is compared the results of Chapters 2 and 3. Just as isolated capacitor storage times shrank with smaller device sizes, the storage times of complete DRAM cells will also decrease. Section 4.3 addresses the scaling behavior of τ_S in complete DRAM cells. Section 4.4 presents variety a of GaAs DRAM cell design issues which are specific to certain physical realizations of the capacitor-transistor DRAM combination. Based on the results of this discussion, some cell designs that are compatible with ion-implanted LSI GaAs FET technologies are proposed and evaluated.

4.1 Experimental Demonstration of a JFET-Accessed DRAM Cell

The epitaxial common N-channel JFET-accessed configuration of Figure 4.1 represented a logical first prototype for a GaAs DRAM cell. The N epilayer provides the channel of the access transistor as well as the N-type storage node of the P^+N junction capacitor. The simple fabrication process is outlined pictorially in Figure 5.3 (Steps 1 - 5), and it is also described in detail on the runsheet given in Appendix 2 (Steps 1 - 35). The

capacitor part of the cell is nearly identical to the P^+NP^- capacitors described in Section 2.12, and the JFET is the same as Figure 3.4 except that no ohmic contact is present at the drain connection to the storage capacitor. The direct N-channel connection to the storage node is advantageous because it eliminates excess drain-to-substrate currents (which could kill DRAM cell storage times) that could arise from ohmic drain contact spiking (Section 3.2.5.1). Furthermore, because the same junctions form the transistor and storage node, the transistor drain leakage should not greatly reduce storage times below those measured on isolated storage capacitors.

4.1.1 Operational Demonstration of the First JFET GaAs DRAM Cell

The physical layout of the first cell tested is given in Figure 4.2, which is nothing more than a more detailed representation of Figure 3.6a. This structure consists of two 100 x 300 μm^2 P^+N junction storage capacitors surrounded by a ring-gate JFET access transistor with $L_{Gate} = 5$ μm. Although only one contact is needed to form a bitline connection, a source and drain contact are included to test the characteristics of the access transistor. These characteristics are given in Figure 4.3, which is merely a reproduction of the 25 °C curve of Figure 3.12.

The charge state of the storage node is determined by measuring the capacitance between the two P^+ capacitor plates. (Measuring the capacitance of a single 200 x 300 μm^2 plate to the substrate would have provided a much weaker signal due to the small series capacitance of the NP^- diode to the substrate.) Unless otherwise specified, the capacitor plates are held at system ground along with the substrate. When the N-region of the storage capacitor is at zero bias, the equilibrium depletion capacitance of the two storage capacitor plates in series is observed representing a logic zero state. When the N-region has been charged to a positive potential representing the logic one state, the reverse bias on the diode junctions drops the measured depletion capacitance.

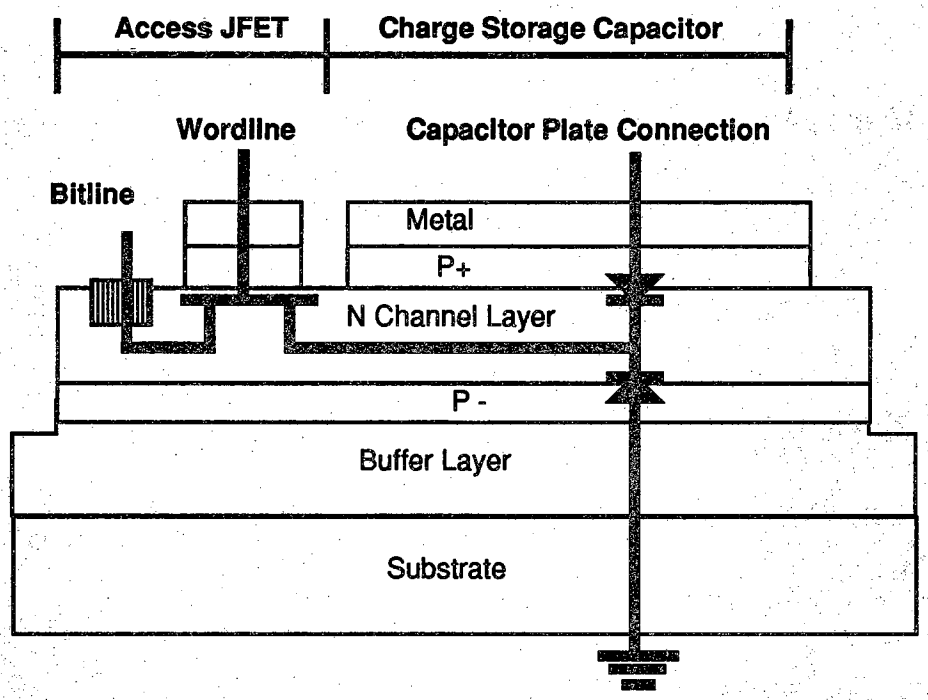


Figure 4.1 Common N-channel epitaxial JFET-accessed GaAs DRAM cell.

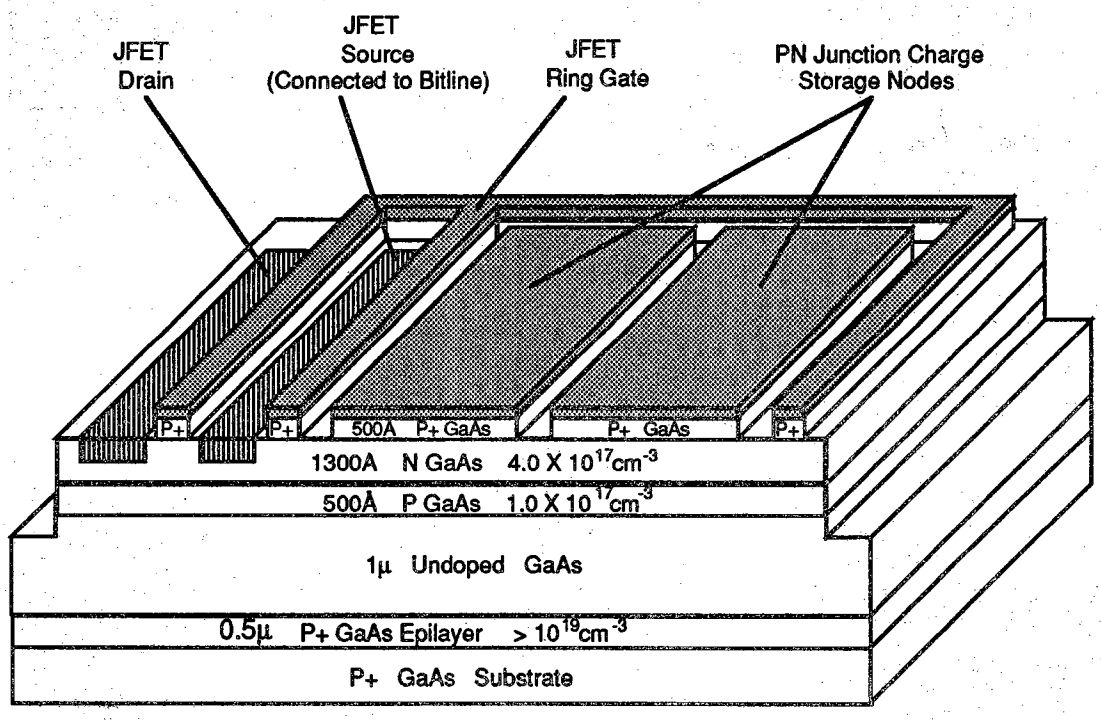


Figure 4.2 Physical realization of the first reported GaAs JFET-accessed 1-T DRAM cell. Device layout is given in Figure 3.6a [3].

The operating voltages $V_{low} = 0$ V, $V_{high} = 0.7$ V, $V_{WL(off)} \leq -1.45$ V, and $V_{WL(on)} = 0$ V were selected with the aid of the arguments of Section 3.5 and the JFET access transistor characteristics of Figure 4.3. To write a logic one, the bitline is taken to $V_{high} = 0.7$ V and the access transistor is turned on by taking the gate to $V_{WL(on)} = 0$ V. Electrons flow from the storage node to the bit-line contact through the turned-on access transistor charging the N storage node to a positive potential. The write cycle is completed by restoring the wordline to $V_{WL(off)} = -1.5$ V prior to the bitline voltage changing away from V_{high}. A logic zero is written to the cell in the same manner, except the bitline is held at $V_{low} = 0$ V instead of V_{high}.

Figure 4.4 shows an experimental demonstration of writing 1's and 0's to the cell via the procedure outlined above. Data are strobed into the cell during 1-ms write pulses applied to the gate of the access transistor. The measured capacitance changes at the time the write pulse is applied, indicating a proper change in the charge-state of the storage node. The fact that the capacitance does not change when the bitline voltage is altered shows that the bitline is sufficiently isolated from the storage node by the turned-off access transistor.

Reading of stored information is demonstrated in Figures 4.5. Here the bit line is monitored by a 0.5 pF active probe as illustrated in Figure 4.5. With the access transistor turned off by $V_G = V_{WL(off)} = -1.45$ V, electrons are removed from the storage node by forward biasing the top capacitor plate junction with a positive bias pulse to pseudo-write a logic one. A short time later the charge state of the cell is sampled by bringing $V_G = V_{WL(on)} = 0$ V to turn on the access transistor connecting the storage node to the bitline. A positive voltage excursion is observed on the bitline as the active probe charge shares with the positively charged storage capacitor. The bit-line voltage decays in about 250 μs due to leakage through the shunt resistance of the probe (Figure 4.5), and this discharges both the probe tip and the storage capacitor. A second read pulse at 3.5 ms shows a much smaller voltage excursion because the storage capacitor was discharged by the previous read operation and now contains a logic zero. The small excursion while reading the logic zero is attributed to charge redistribution during the positive voltage swing of V_G, as some electrons are sucked from the bitline to fill the shrinking gate depletion. In a

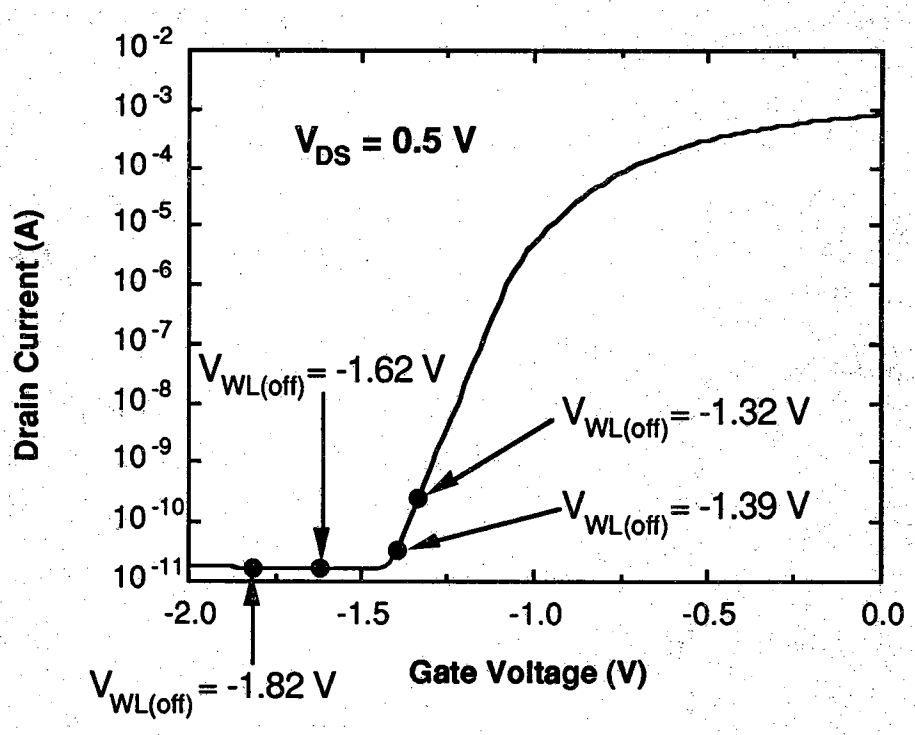


Figure 4.3 JFET DRAM cell access transistor I_D versus V_{GS} characteristics. This was taken from the 5 x 350 μm^2 ring-gate device of Figure 4.2. Device parameters: V_{T0} = -1.0 V, n_{Sub} = 1.25, I_{DMin} = 16 pA at V_G = -1.45 V.

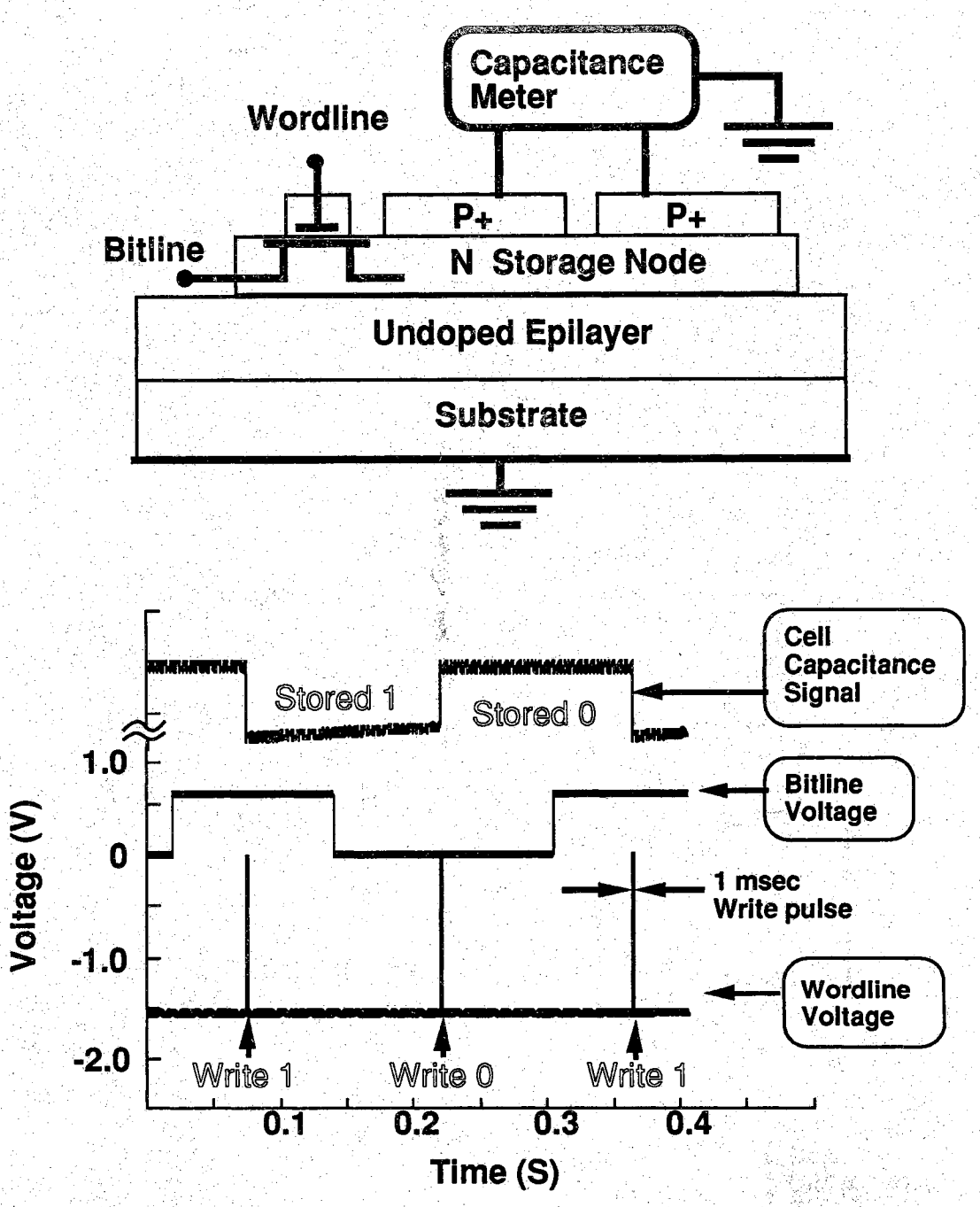


Figure 4.4 Demonstration of the write capability of the JFET DRAM cell. Note that the capacitance changes at the time of the 1-ms wordline (gate) pulse in accordance with the voltage applied to the bitline contact. This data was taken at room temperature in the dark on the DRAM cell of Figure 4.2.

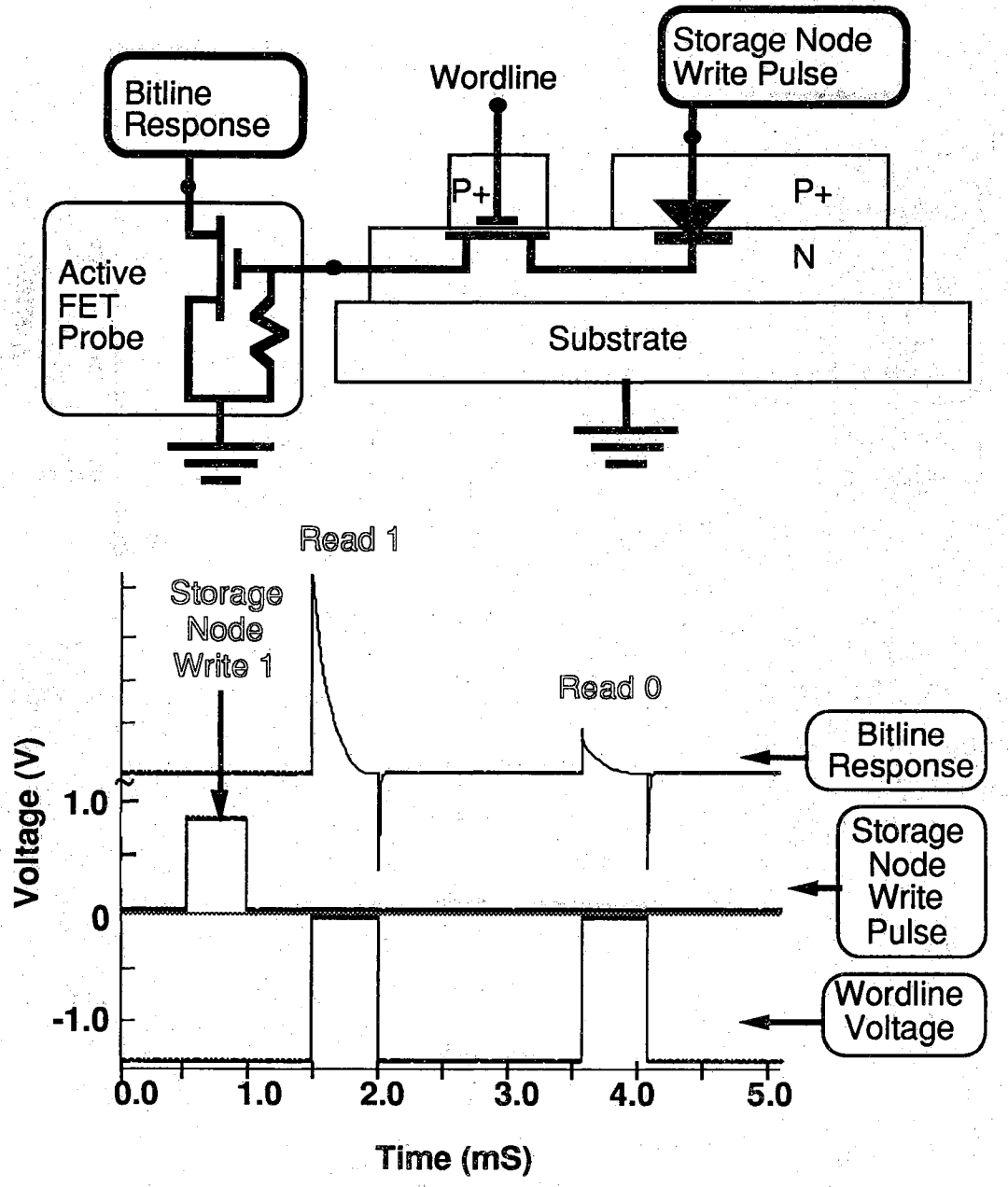


Figure 4.5 Demonstration of the read capability of the JFET DRAM cell. The potential of the bitline is monitored by a 0.5 pF active probe, which electrically behaves like a DRAM array bitline during a sense cycle. See text for further explanation.

complete integrated circuit implementation, sense amplifiers would account for this in detecting and latching the data for readout [57].

4.1.2 JFET DRAM Cell Storage Time and Leakage Mechanisms

The gradual decay of capacitance in Figure 4.4 following a stored one is due to electrons repopulating the storage node through various leakage mechanisms. These mechanisms, which are pictorially outlined in Figure 4.6, have all been documented in previous sections of this dissertation. The leakages denoted by 1 and 2 are the reverse-biased PN junction mechanisms of Chapter 2, while the leakages labelled by 3 and 4 are FET subthreshold drain-to-source and drain-to-gate conduction (Chapter 3). Since the drain of the access transistor is the same as the storage node, the FET drain-to-substrate leakage (Section 3.2.5, Figure 3.9) is considered part of leakage 2. There is no capacitance transient observable in Figure 4.4 after the storing of a logic zero, since this is the equilibrium condition for the cell.

To more thoroughly study the access transistor leakage mechanisms, the series of capacitance recovery transients in Figure 4.7 were taken at room temperature. Using the procedure outlined previously, a logic one (V_{high} = 0.5 V) is written to the cell at time t = 0, and then allowed to decay with the bitline having been immediately restored to an idle value of V_{low} = 0 V. The difference between the transients is that the cell was operated with varying wordline off voltages ($V_{WL(off)}$ = -1.32, -1.39, -1.62, and -1.82 V as shown in Figure 4.3). The behavior of the transients as a function of $V_{WL(off)}$ roughly matches the subthreshold drain leakage of Figure 4.3 as a function of V_G. When $V_{WL(off)}$ isn't negative enough (as is the case for $V_{WL(off)}$ = -1.32 V), access transistor source-to-drain conduction (leakage 3 of Figure 4.6) governs DRAM cell storage time. However when the cell is properly biased ($V_{WL(off)}$ < 1.45 V), reverse-biased PN junction leakage mechanisms determine cell storage time.

A variation of the timestep technique of Section 2.3.5 was used to simulate DRAM cell capacitance recovery transients and storage times. The leakage components of Figure 4.3 can each be modelled or measured

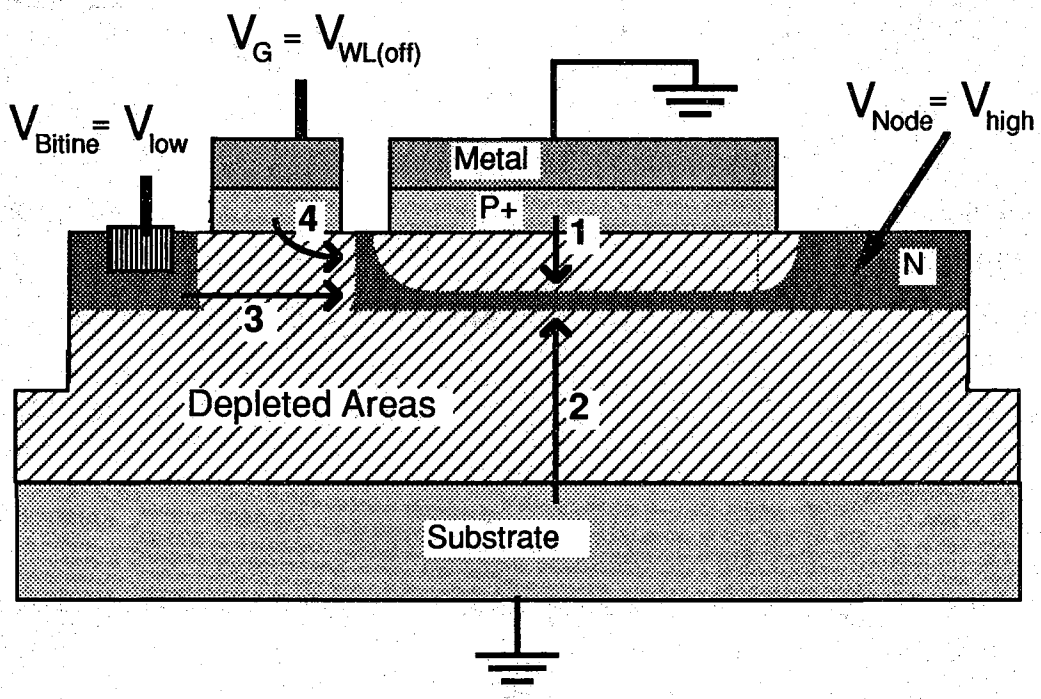


Figure 4.6 JFET-accessed DRAM cell leakage mechanisms that cause discharge of a stored one. Leakages 1 and 2 are the reverse-biased PN junction storage capacitor leakages presented in Chapter 2, while leakages 3 and 4 are the subthreshold FET drain leakage mechanisms presented in Chapter 3.

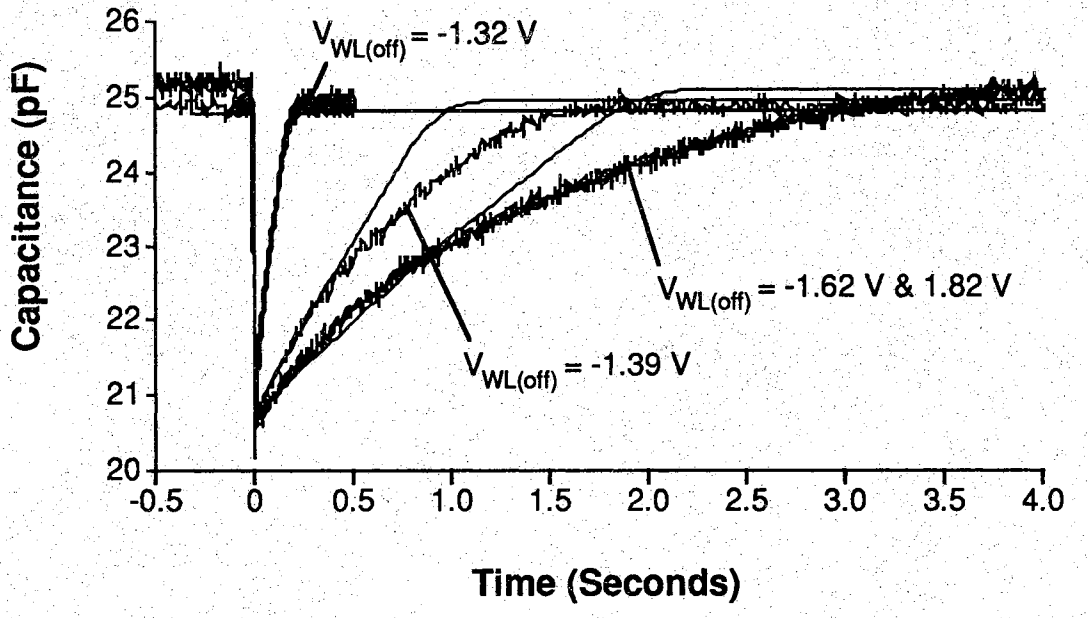


Figure 4.7 JFET DRAM cell capacitance recovery transients as a function of wordline off voltage. A logic one is written to the JFET DRAM cell of Figure 4.2 and then allowed to decay. The exact procedure used is as follows: At t = 0 the access transistor is turned on for 5 msec by taking V_G to $V_{WL(on)} = 0$ V with the bitline at $V_{high} = 0.5$ V. 2 msec after V_G is restored to $V_{WL(off)}$ (value specified in the figure), the bitline is restored to $V_{low} = 0$ V. The thin lines represent calculations based on measured DC leakage currents, as discussed in the text [3].

as a function of voltage, and these leakages in turn can be summed to provide the total current flowing into the storage node as a function of the voltages present in the DRAM cell. The storage node charge after a timestep Δt was calculated via (2.40) and (2.41), and the corresponding new storage node voltage was applied to the leakage current calculations for the next timestep. Simulations of this nature were carried out for the JFET-accessed DRAM cell based on measured cell I-V characteristics, and the results are given by the thin lines of Figure 4.7 [3].

In this particular device it appears that leakage from the capacitor itself is the primary limiting factor, but gate-to-drain FET leakage cannot be classified as completely inconsequential. The plot of Figure 4.8 shows the measured 1/e storage time performance of the JFET-accessed DRAM cell along with data taken from an isolated P^+NP^- storage capacitor on the same die. Consisting of a mesa with two 100 x 300 μm^2 top capacitor plates, the isolated storage capacitor has almost the same lateral dimensions and cross-section as the storage node of the DRAM cell. The minute difference between the isolated capacitor and complete DRAM cell storage times suggests that the properly-biased access transistor leakage is smaller than the storage capacitor leakage. This fact is not really surprising when one considers the experimental results of Chapter 2. Both capacitors have large areas of surface-exposed N-regions, and both have a large generation volume in the lightly-doped material beneath the N-layers. The fact that the capacitor and the DRAM cell show both show an activation energy somewhat less than half the zero-temperature bandgap ($E_{GE0}/2 = 0.79$ eV) is consistent with the surface-exposed capacitor behavior documented in Section 2.9.

4.2 Experimental Demonstration of MESFET-Accessed DRAM Cells

Figure 4.9 shows a cross-section of the recess-etched epitaxial MESFET DRAM cells that were investigated. The cell features a MESFET access transistor directly connected to a P^+iN^+ storage capacitor, and it is fabricated with 5 masking steps described in Appendix 1 and Figure 4.10.

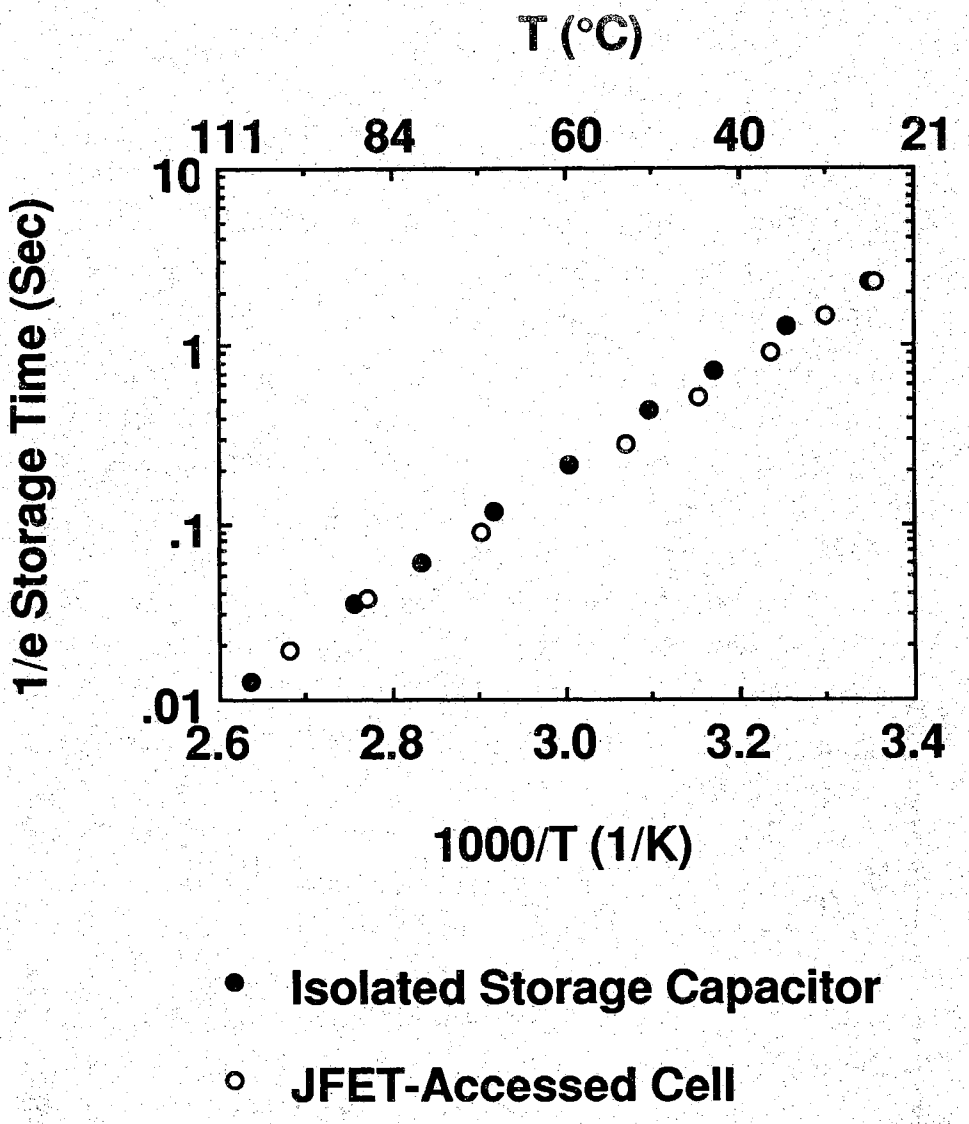


Figure 4.8 Comparison of isolated capacitor and JFET DRAM cell storage times. The isolated capacitor has the same dimensions as the DRAM cell capacitor, and was located adjacent to the DRAM cell on the wafer. The positive charge was written to the isolated capacitor with a 1-V, 1-ms pulse, while a V_{high} = 0.5 V was the DRAM cell using the write one technique previously described with $V_{WL(off)}$ = -1.7 V (see text and caption of Figure 4.7). The activation energy for the isolated capacitor is E_A = 0.60 eV, while the DRAM cell activation energy is E_A = 0.63 eV.

One of the main advantages of this configuration over the JFET configuration of Section 4.1 is that the N-layer profiles of the access transistor and storage capacitor can be optimized separately. The charge density and available logic swing of the storage capacitor are maximized by the heavily-doped N^+ layer, while the threshold voltage of the access transistor can be set independently by the depth of the recess-etch.

The MESFET-accessed cell is read and written in the same manner as the JFET-accessed cell of the previous section. The only change is that the operating voltages must be adjusted to match the I_D versus V_{GS} characteristics of the MESFET's in question. Figure 4.11 demonstrates the write operation of a MESFET-accessed DRAM cell, whereby the writing of 1's and 0's to the cell is monitored by measuring the storage node capacitance. In this particular case the operating voltages were chosen to demonstrate the pseudo-enhancement access scheme of Section 3.5.3, whereby $V_{WL(off)} = 0$ V to eliminate undesired substrate-to-gate current in the storage state. When V_{low} is shifted away from ground, it is advantageous (but not necessary in all cases) to bias the top capacitor plate connection at V_{low}. This decreases the voltage drop across the top capacitor junction resulting in reduced leakage and slighly increased charge storage density (Figure 2.4).

An active-probe measurement, similar to what was carried out on the JFET cell in Section 4.1.1, verified the read operation of MESFET-accessed DRAM cells (Figure 4.12). The difference in the bitline response between a read 1 and a read 0 is evident in the initial response of the bitlines. After the charge has decayed through the shunt resistance of the probe with the wordline is still on, the effect of the forward-biased gate on the bitline can be witnessed by the positive plateau in the active probe signal. The degree to which V_G controls the bitline potential is not surprising when one considers that $V_{WL(on)} = 0.5$ V barely satisfies (3.12) for an assumed MESFET $V_{GM} = 0.6$ V. The result suggests that that V_{GM} is closer to 0.5 V for this particular MESFET (see Sections 3.5.1.1 and 3.5.2).

An effort was made to document high-speed cell operation, but the results were inadequate due to testing equipment limitations. The write speeds of the MESFET-accessed DRAM cells were tested by decreasing the

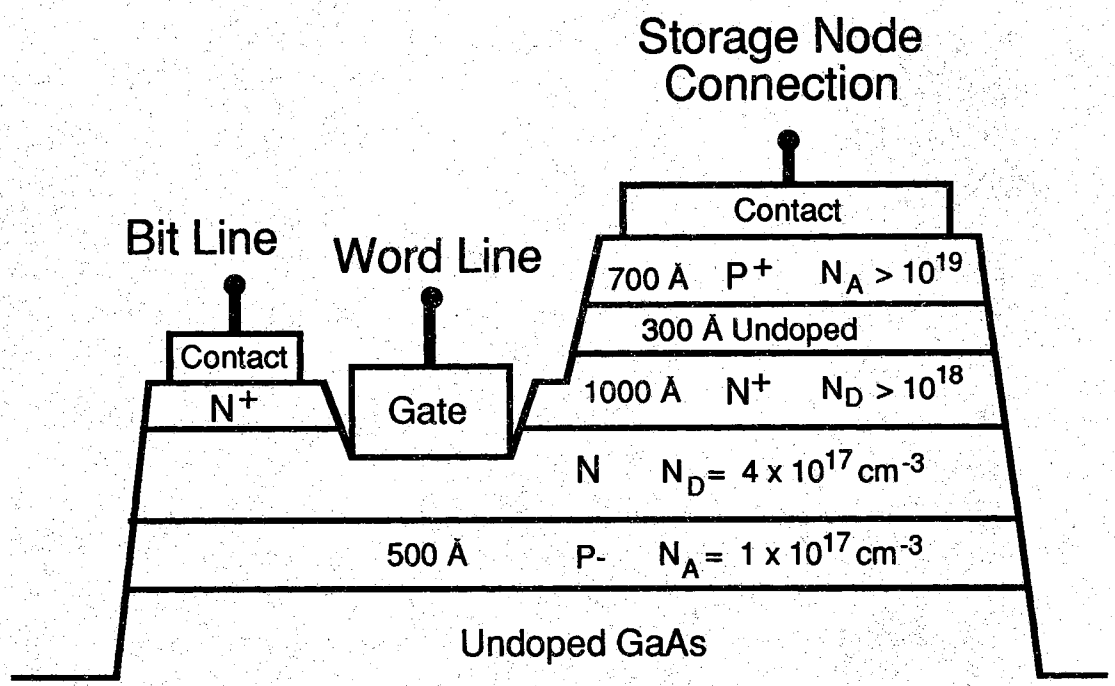
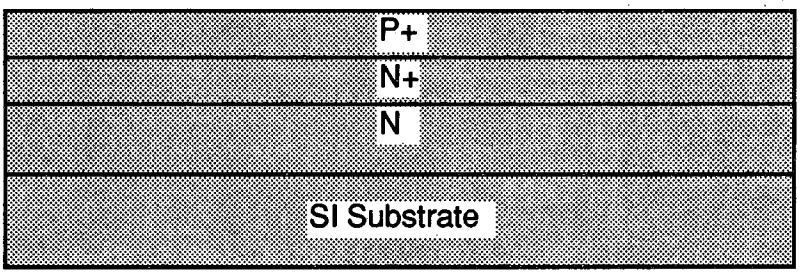
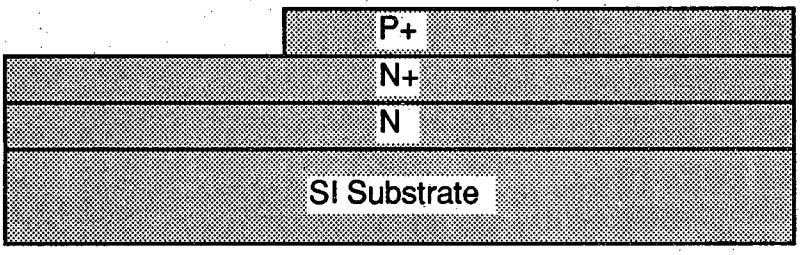


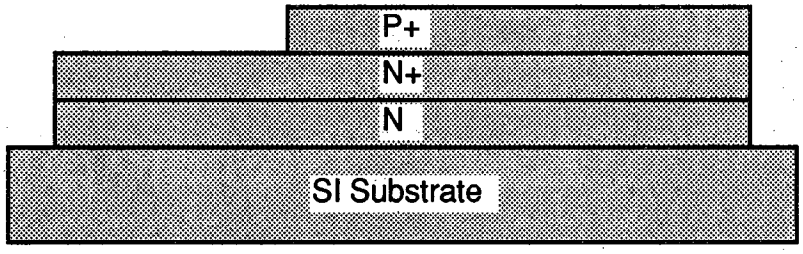
Figure 4.9 Recess-etched epitaxial MESFET DRAM cell. The thickness of the N-channel beneath the gate is set by a recess etch. The target thickness was approximately 800 Å, but there was deviation that was witnessed by threshold voltage variations between wafer lots.



Step 1: Grow Film on Semi-Insulating Substrate.

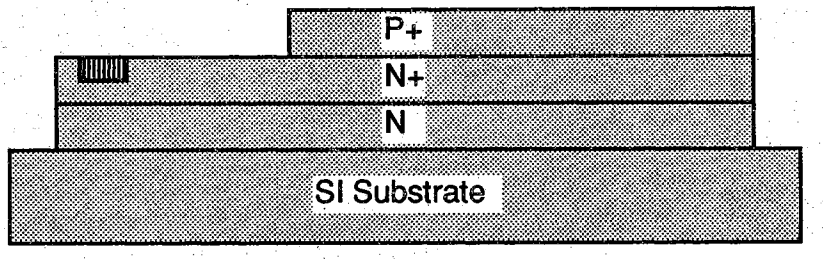


Step 2: Suface Exposure Etch.

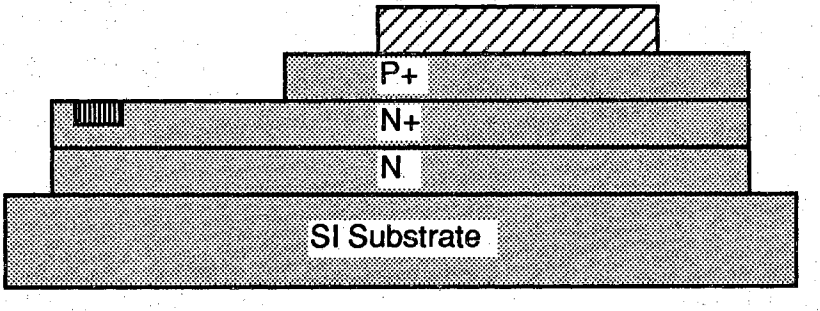


Step 3: Mesa Etch.

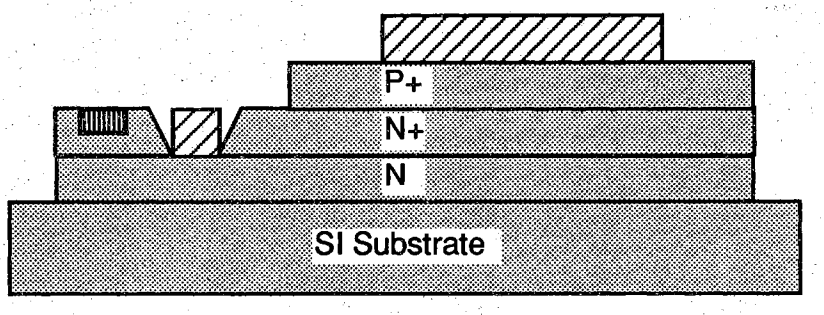
Figure 4.10 Epitaxial MESFET-accessed DRAM cell process sequence. The correct epilayers are given in Figure 4.9, as some have been omitted from this figure for clarity.



Step 4: Ohmic Contact Deposition and Alloy.



Step 5: Capacitor Plate Contact Deposition.



Step 6: Gate Recess Etch and Deposition.

Figure 4.10, continued

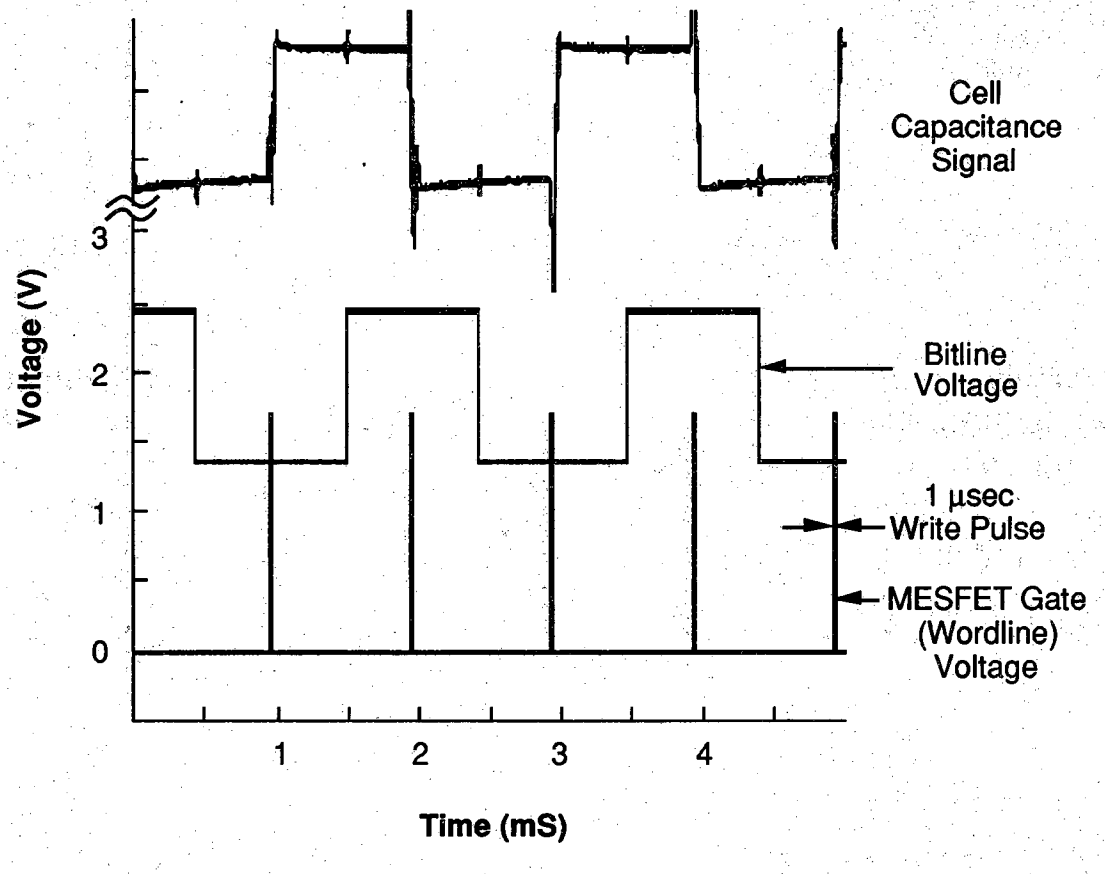


Figure 4.11 Demonstration of the write capability of an epitaxial MESFET DRAM cell using a pseudo-enhancement-access operating voltage scheme. The logic levels are shifted positive so that $V_{WL(off)} = V_{Subs} = 0$ V (see Section 3.5.3), and $V_{T0} \cong -0.8$ V for this device. The layout of this DRAM cell is the 10 x 200 μm^2 non ring-gate geometry given in Figure 4.14.

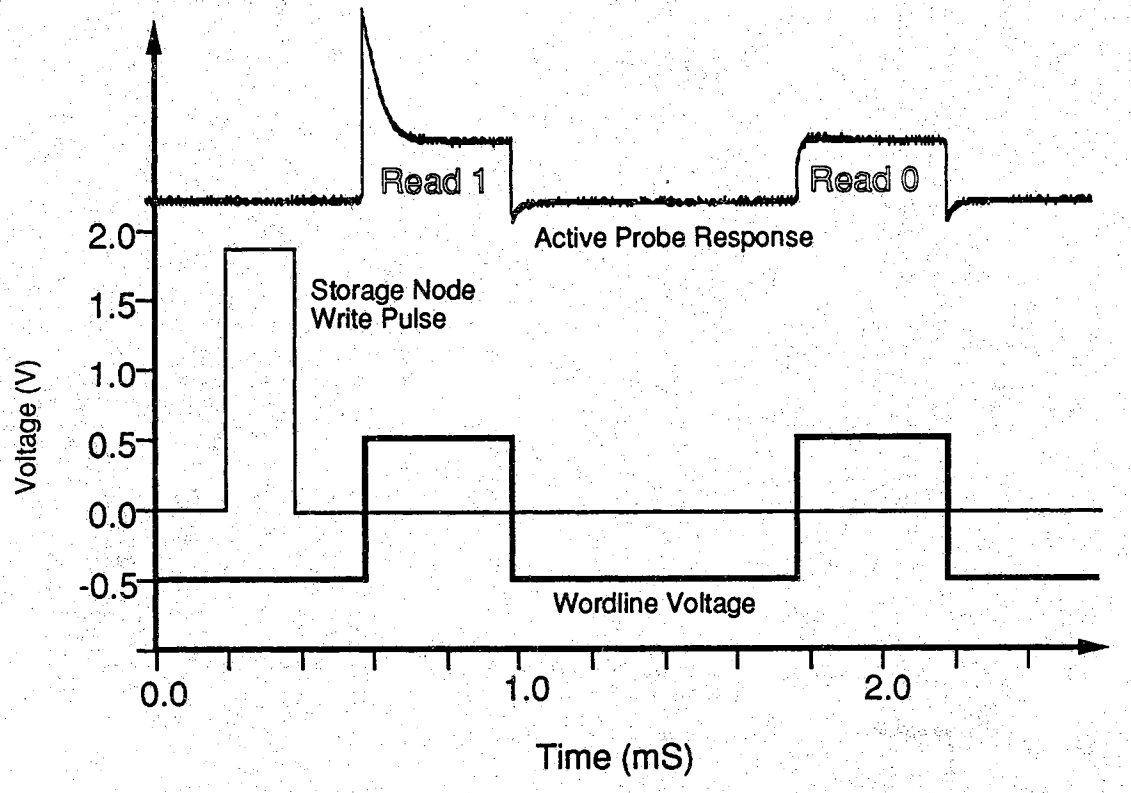


Figure 4.12 Demonstration of the read capability of an epitaxial MESFET-accessed DRAM cell. The potential of the bitline is monitored by a 0.5 pF active probe, which electrically behaves like a DRAM array bitline during a sense cycle. The measurement procedure is the same as that outlined in Section 4.1.1 for the JFET read measurement of Figure 4.5, except that different operating voltages are employed as depicted above. The device tested in this figure has a $V_{T0} \cong 0.1$ V, and a layout geometry like Figure 4.17 with $L_{Gate} = 2$ μm. The positive bitline excursion for the read 0 cycle is due to current drawn by the forward-biased Schottky gate.

pulse width of the $V_{WL(on)}$ write pulses in Figure 4.11. The cells functioned at pulse widths of 20 ns, which was the the minimum pulse width obtainable on the experimental setup. Figure 4.13 shows a blow-up of the leading edge of the "read 1" bitline excursion of Figure 4.12. The delay between the start of the wordline pulse and the start of the active probe excursion is attributed to an inadvertent difference in apparatus cable length. The rise of the active probe on the bitline parallels the wordline voltage rise on the timescale shown, and the magnitude of the rise is comparable to the size of the "read 1" excursion in Figure 4.12. These waveforms suggest a read access time of less than 20 ns, but this is well above the near-nanosecond read access speed believed obtainable (from SPICE simulations) in the cell structure measured.

4.2.1 MESFET DRAM Cell Leakages and Storage Times

The results of Chapters 2 and 3 suggest that thermionic reverse leakage of the Schottky gate-to-drain diode will dominate the storage time of the conventional MESFET-accessed DRAM cell, and this is strongly supported by the experimental evidence. Recall the comparison of Figure 3.7 whereby I_{DMin} of a PN junction gate JFET was well over a hundred times smaller than I_{DMin} in a comparable Schottky gate MESFET. Since the benchmark device for this comparison was the ring-gate FET/DRAM cell structure of Figure 3.6a, a direct comparison of DRAM cell storage times can also be drawn provided proper operating voltages are employed to put $V_{WL(off)} \leq V_G(I_{DMin})$ in both devices. The L_{Gate} = 10 μm MESFET version of the DRAM cell of Figure 3.6a showed a 1/e storage time of just 2.4 msec at room temperature, compared to 2.3 seconds for the L_{Gate} = 5 μm JFET version of the cell of Figure 3.6a.

The example given above paints a pretty bleak picture for MESFET-accessed cells, but much better storage time results are obtainable through use of intelligent cell geometries and optimization of Schottky gate metallization techniques. Along the lines of general arguments presented in Chapter 2, the storage time will depend on the magnitude of the leakage currents relative to the charge stored in the cell. The stored charge is

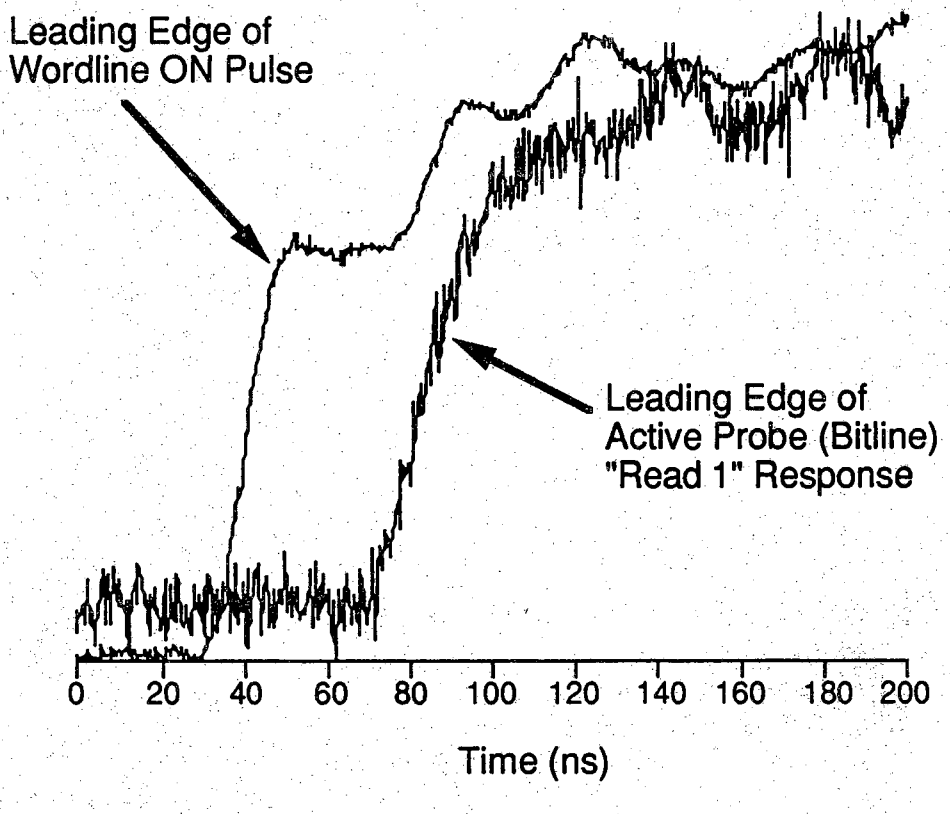


Figure 4.13 Close-up of the leading edge of the "Read 1" active probe response. To better compare the rising edge response, the waveforms are normalized. Most of the delay between the rising edge of the wordline pulse and the rising edge of the active probe response is attributed to an inadvertent difference in apparatus cable length.

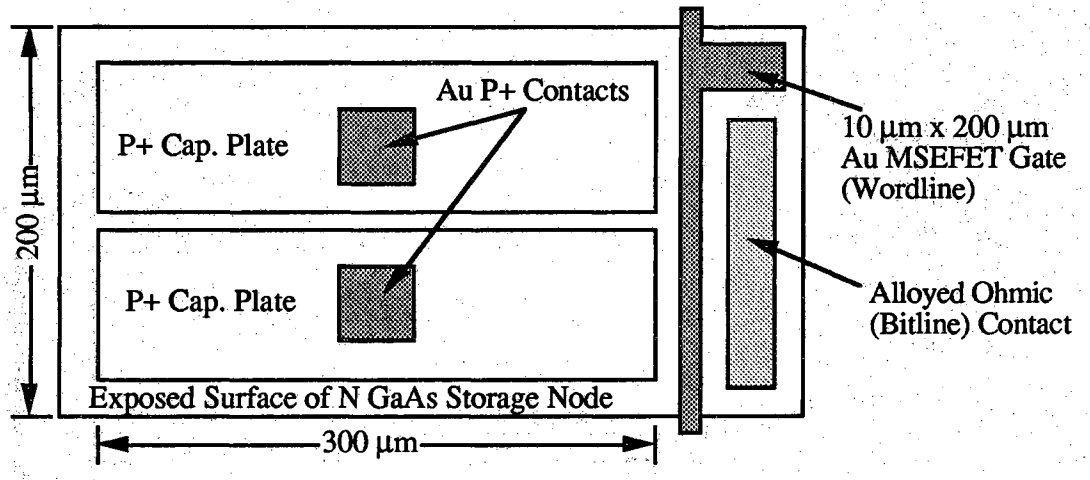


Figure 4.14 Large non-ring-gate MESFET-accessed test DRAM cell.

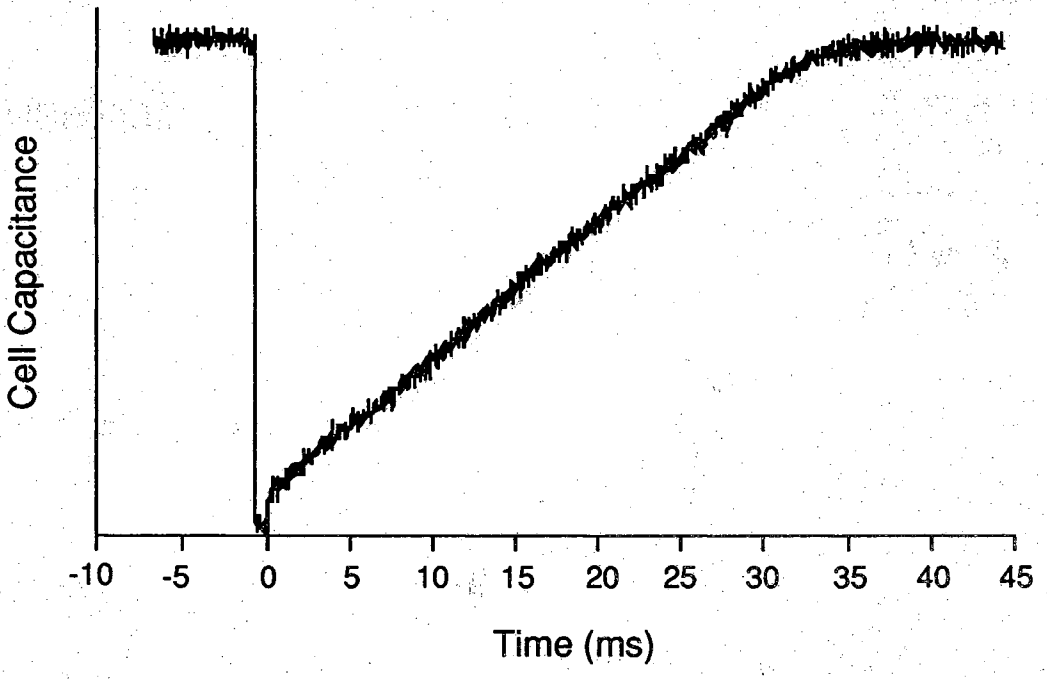


Figure 4.15 Write one recovery transient taken from the MESFET DRAM cell of Figure 4.14. A logic one is written to the cell at t=0 and allowed to recover. The procedure is similar to that outlined in 4.7, with V_{low} = 0 V, V_{high} = 0.5 V, $V_{WL(off)}$ = -0.2 V, and $V_{WL(on)}$ = 0.5 V. MESFET V_T is approximately 0.2 V.

proportional to the capacitor area, while the gate leakage is proportional to the size of the gate. Since gate leakage dominates the storage time of conventional MESFET DRAM cells, the above argument suggests that cutting the area and perimeter of the gate relative to the storage node should result in storage time gains. A qualitative trend in this direction was noted in data taken from devices with varying lateral geometries, but due to scatter in the limited number of devices measured, a quantitative relationship was never established experimentally. Figure 4.15 shows a storage time transient taken from a the MESFET DRAM cell of Figure 4.14. The storage capacitor is the same size as the ring-gate device of Figure 3.6a, but the reduced access transistor gate size results in a larger 1/e storage time of 21 msec.

The non-exponential capacitance recovery transient of Figure 4.15 belies the FET-dominated nature of leakage that restores the storage node to equilibrium. Recalling the derivation of Section 2.3.1, the exponential charge recovery of isolated PNP capacitors was due the fact that the leakage current and charge are closely related through (2.27) and (2.28). In FET-leakage dominated DRAM cells however this coupling is destroyed, as the access transistor determines the leakage while the capacitor determines the charge. Measurements and timestep simulations reveal that the shape of the recovery transient largely depends on the response of access transistor leakage to changes in the storage node voltage. In cases where the change in storage node voltage causes little change in access transistor leakage, the recovery transient becomes nearly linear (like Figure 4.15).

4.2.2 $(NH_4)_2S$-Treated MESFET DRAM Cell

In Section 3.2.4 it was demonstrated that MESFET Schottky gate-to-drain leakage could be dramatically reduced by properly employing an ammonium-sulfide pretreatment just prior to Au-gate metallization. The technique was applied to MESFET-accessed DRAM cells using the procedure outlined in Section 3.2.4 [8,9,15]. Figure 4.16 illustrates the increase in storage time observed on the non-ring-gate structure of Figure

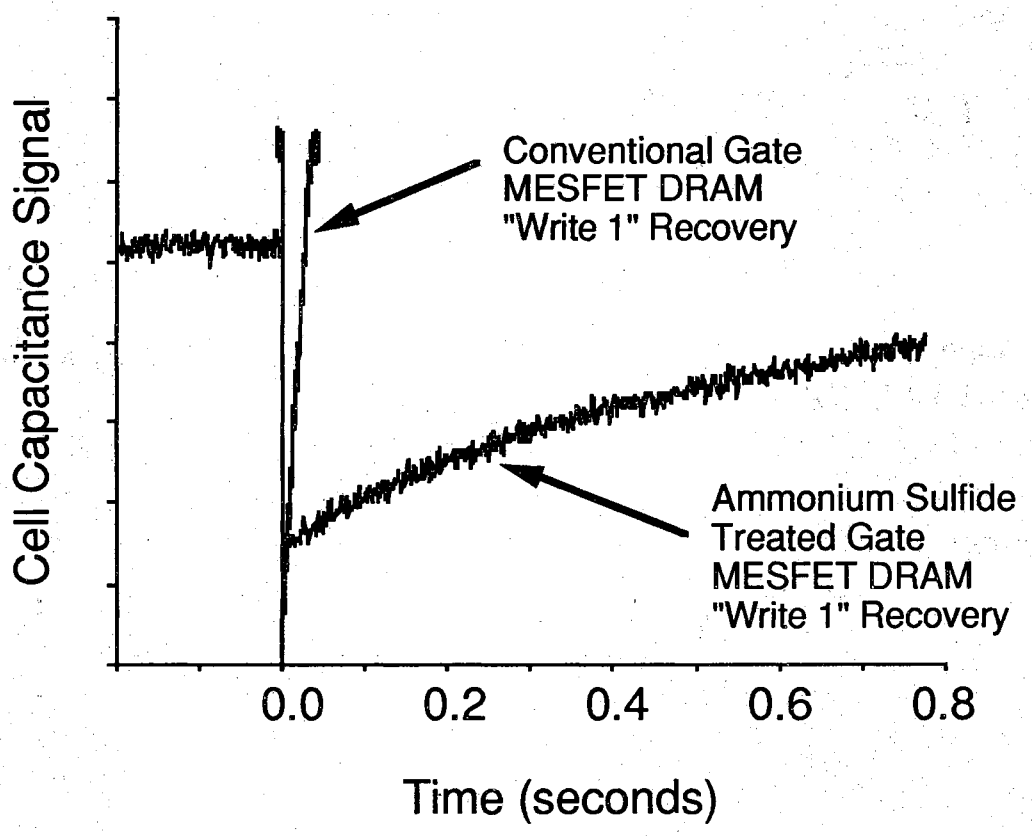


Figure 4.16 Comparison of write one recovery transients between conventional gate and $(NH_4)_2S$-treated gate MESFET DRAM cells. The cell layout of Figure 4.14 is used as the basis of comparison, and the operating voltages are as described in Figure 4.15. The conventional gate curve is the transient presented in Figure 4.15 on a different time scale.

4.14. Following the writing of a logic one to the cell, the untreated cell decays to the 1/e point in 21 msec while the $(NH_4)_2S$-treated DRAM cell has a storage time of one second. A similar improvement was obtained in the ring-gate geometry of Figure 3.6a, as storage time jumped from 2.4 msec to 137 msec. This dramatic increase in storage time due to decreased MESFET Schottky gate leakage appears to be permanent, as the devices have not degraded over the period of one year's storage in ordinary room air.

4.3 Cell Storage Time Scaling Issues

In Chapter 2 the storage times of PNP capacitors varied with lateral device geometry due to the fact that the leakage current didn't scale on a one-to-one basis with the charge stored in the device. The presence of significant perimeter-scaled leakage results in significant storage time degradation as PNP capacitors are shrunk to useful sizes. The same problem exists in shrinking the GaAs DRAM cells to practical sizes, but the situation is more complicated due to the presence of additional leakage sources. An assessment of DRAM cell scaling behavior requires proper consideration of all leakages present in the cell relative to the charge in the storage node. Although more exact measurements and calculations are warranted (Section 6.1.4), the general DRAM cell τ_S scaling behavior can be understood through a variation of the storage time approximation of Section 2.3.4.

Consider the FET-accessed DRAM cell designs demonstrated in Sections 4.1 and 4.2. The charge stored in the P^+NP^- capacitor immediately after the writing of a logic one (V_{high}) is given by:

$$Q(t=0^+) = qN_DA[W(V_{high}) - W(V_{low})] \qquad (4.1)$$

This formula is analogous to Chapter 2 diode capacitor charge expressions, except that the zero-bias depletion width has been replaced with $W(V_{low})$ to reflect the possible use of positively shifted logic levels (Section 3.5.2). If

leakages 3 and 4 in Figure 4.6 were always insignificant compared to leakages 1 and 2, complete DRAM cells would show the same storage time behavior as comparable isolated storage capacitors. As Figure 4.8 shows, this is nearly the case for the JFET-accessed cell of Section 4.1. The capacitor storage time is estimated by:

$$\tau_{SCap} \cong \frac{Q(t=0^+)\left(1 - \frac{1}{e}\right)}{I_{RTop}(V_{high}) + I_{RBot}(V_{high})} = \frac{Q(t=0^+)\left(1 - \frac{1}{e}\right)}{I_{Cap}} \qquad (4.2)$$

where I_{Cap} is the sum of the top and bottom capacitor diode junction leakages I_{RTop} and I_{RBot} seen at storage node bias V_{high}.

If the transistor leakages are dominant, as is the case with the conventional-gate MESFET DRAM's of Section 4.2, the cell storage time can be estimated to first order by applying the access transistor subthreshold current characteristics to a variation of (2.39):

$$\tau_{STran} \cong \frac{Q(t=0^+)\left(1 - \frac{1}{e}\right)}{I_D(V_G = V_{WL(off)}, V_{DS} = V_{high} - V_{low})} = \frac{Q(t=0^+)\left(1 - \frac{1}{e}\right)}{I_{Tran}} \qquad (4.3)$$

This formula is valid only when the drain current minimum measured on a given FET accurately reflects the current seen by the storage node of a corresponding DRAM cell. For example, (4.3) does not apply between a directly-connected JFET DRAM cell (Figure 4.1) and the measured drain characteristics of Figure 3.11, because the measured I_{DMin} in Figure 3.11 is determined by alloy contact spiking that is not present in the directly-connected DRAM cell.

Combining the above results one can estimate the DRAM cell storage time τ_{SCell} as:

$$\tau_{SCell} \cong \frac{Q(t=0^+)\left(1 - \frac{1}{e}\right)}{I_{Cap} + I_{Tran}} \qquad (4.4)$$

To first order, (4.4) suggests that transistor leakage measurements and storage capacitor measurements can be combined to obtain an approximation for the storage time of a complete DRAM cell:

$$\frac{1}{\tau_{SCell}} = \frac{1}{\tau_{SCap}} + \frac{1}{\tau_{STran}} \qquad (4.5)$$

where τ_{SCap} is the measured storage time of an analogous isolated capacitor structure and τ_{STrans} is calculated from (4.2) using access transistor leakage data.

Table 4.1 compares measured DRAM cell storage times with storage times crudely extrapolated from measured isolated capacitor and FET characteristics. The ring-gate FET/DRAM devices (Figure 3.6a) described in Sections 4.1 and 4.2 are presented. Although the capacitor layout is essentially the same, the disparity in initial cell charge $Q(t=0^+)$ is due to the difference in doping profiles and logic high voltages used in the respective measurements (JFET V_{high} = 0.5 V while MESFET V_{high} = 1.25 V). I_{Tran} at $V_{WL(off)}$ is estimated from the measured subthreshold characteristics of Figures 3.12 and 3.14, and (4.3) is used to calculate a corresponding τ_{STran}. Isolated storage capacitors of the correct size were measured, and τ_{SCap} is combined with τ_{STran} through (4.5) to produce a crude estimate for τ_{SCell}. It should be emphasized that Table 4.1 represents only a thumbnail comparison, because several voltage-dependent factors are ignored or estimated in the procedure outlined above.

Table 4.1 Comparison of roughly estimated and measured DRAM cell storage times. This table represents an imprecise comparison due to the fact that several factors are estimated (see text).

Device	$Q(t=0^+)$	I_{Tran}	Estimated τ_{STran}	Measured τ_{SCap}	Estimated τ_{SCell}	Measured τ_{SCell}
MESFET	110 pC	20 nA	3.5 ms	1.4 s	3.5 ms	2.4 ms
JFET	45 pC	17 pA	1.7 s	2.4 s	1 s	2.3 s

The storage time scaling behavior of capacitors was documented in Chapter 2, while access transistor leakages were addressed in Chapter 3. Knowing the scaling behavoir of all cell leakage components, the storage time scaling behavior of small-geometry DRAM cells can be extrapolated using (4.1) through (4.5). For this discussion, the generalized DRAM cell geometry of Figure 4.17 is assumed. A square diode-junction storage capacitor is directly connected to an N-channel access FET with $L_{Cap} = W_{Cap}$, and the entire structure rests on a lightly-doped substrate. Because the FET drain-to-substrate diode is the same as the storage node-to-substrate diode, I_{DSub} of the FET is considered to be part of the underlying junction capacitor leakage. The cell charge in (4.1) scales with top capacitor junction area A_{Cap}, and can be re-expressed as:

$$Q(t=0^+) = \rho_{Cap} A_{Cap} \tag{4.6}$$

where ρ_{Cap} is the charge density corresponding to the logic levels and capacitor doping profile chosen. In a square capacitor layout of Figure 4.17 with $L_{Cap} = W_{Cap}$ the charge in (4.6) becomes:

$$Q(t=0^+) = \rho_{Cap} W_{Cap}^2 \tag{4.7}$$

The leakage from the capacitor can be written as the sum of the top and bottom junction leakages:

$$I_{Cap} = I_{TopCap} + I_{BotCap} \tag{4.8}$$

As discussed in Chapter 2, the capacitor diode leakages can be expressed as:

$$I_{TopCap} = J_{ATopCap} A_{TopCap} + J_{PTopCap} P_{TopCap} \tag{4.9}$$

$$I_{BotCap} = J_{ABotCap} A_{BotCap} + J_{PBotCap} P_{BotCap} \tag{4.10}$$

where $J_{ATopCap}$ and $J_{ABotCap}$ are the area-scaled leakage current densities (A/cm^2), $J_{PTopCap}$ and $J_{PTopCap}$ are the perimeter-scaled leakage current

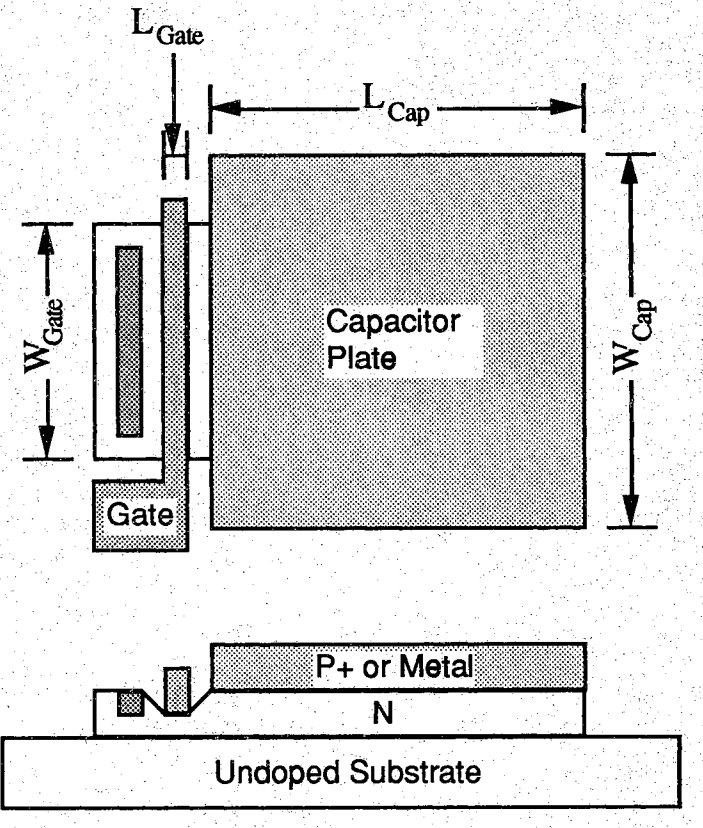


Figure 4.17 Generalized GaAs DRAM cell structure. For the storage time scaling model developed in the text, $W_{Cap} = L_{Cap}$ and $W_{Gate} = K_{GC}W_{Cap}$. The model is fully applicable to any gate/capacitor combination of PN/Schottky diodes.

densities (A/cm), and A_{TopCap}, A_{BotCap}, P_{TopCap}, and P_{BotCap} are the areas and perimeters of the top and bottom storage capacitor diode junctions. The lateral geometries of top and bottom capacitor junctions in Figure 4.17 are almost the same, so $A_{TopCap} \cong A_{BotCap} = A_{Cap}$ and $P_{TopCap} \cong P_{BotCap} = P_{Cap}$. This allows the capacitor current densities in (4.9) and (4.10) to be lumped together:

$$I_{Cap} = J_{ACap} A_{Cap} + J_{PCap} P_{Cap} \tag{4.11}$$

where

$$J_{ACap} = J_{ATopCap} + J_{ABotCap} \tag{4.12}$$

$$J_{PCap} = J_{PTopCap} + J_{PBotCap} \tag{4.13}$$

In a square capacitor layout of Figure 4.17:

$$\frac{P_{Cap}}{A_{Cap}} = \frac{4\,W_{Cap}}{W_{Cap}^2} = \frac{4}{W_{Cap}} \Rightarrow P_{Cap} = \frac{4}{W_{Cap}} A_{Cap} \tag{4.14}$$

The substitution of (4.14) into (4.11) leads to:

$$I_{Cap} = \left[J_{ACap} + \frac{4\,J_{PCap}}{W_{Cap}} \right] A_{Cap} = J_{ACap} W_{Cap}^2 + 4\,J_{PCap} W_{Cap} \tag{4.15}$$

In a properly designed access transistor, I_{DS} is shut-off at $V_{GS} = V_{WL(off)}$ leaving I_{DG} as the chief transistor leakage (Chapter 3). The scaling behavior of I_{DG} was not directly measured in Chapter 3 due to interference from other transistor leakage sources, but the leakage FET gate diode under reverse bias scales similar to the diodes of Chapter 2. Depending upon the relative importance of bulk- and perimeter-scaled leakage mechanisms, the FET gate diode leakage will scale with some combination of gate area (A_{Gate}) and gate perimeter (P_{Gate}):

$$I_{Tran} = J_{AGate} A_{Gate} + J_{PGate} P_{Gate} \qquad (4.16)$$

In terms of the Figure 4.17 gate dimensions W_{Gate} and L_{Gate}, (4.16) can be re-written as:

$$I_{Tran} = J_{AGate} L_{Gate} W_{Gate} + J_{PGate}(2L_{Gate} + 2W_{Gate}) \qquad (4.17)$$

Considering the need for high-speed access transistor operation, the aspect ratio W_{Gate}/L_{Gate} would in all likelihood be large enough that (4.17) approximates to:

$$I_{Tran} = J_{AGate} L_{Gate} W_{Gate} + 2J_{PGate} W_{Gate} \qquad (4.18)$$

Considering the DRAM cell of Figure 4.17, the perimeter leakage on the bitline side of the gate shouldn't discharge the storage node. Therefore the factor of 2 from the perimeter term of (4.18) can be dropped resulting in:

$$I_{Tran} = [J_{AGate} L_{Gate} + J_{PGate}] W_{Gate} \qquad (4.19)$$

Reasonable approximations for the area and perimeter leakage components of the gate diode can be obtained from diode or PNP capacitor measurements (Chapter 2).

When viewed in a loose empirical sense, (4.19) can be used to model more than just FET gate-to-drain diode leakage. If source-to-drain subthreshold leakage is significant for a specified submicron gate length, the increased I_{DS} leakage can be incorporated into (4.19) by increasing J_{PGate} accordingly. However the modified J_{PGate} would no longer correspond to the perimeter current density obtained from straightforward I-V measurements taken on corresponding diode structures.

Incorporating (4.7), (4.15), and (4.19) into the storage time estimate of (4.4):

$$\tau_{SCell} \cong \frac{\rho_{Cap} W_{Cap}^2 \left(1 - \frac{1}{e}\right)}{[J_{ACap} W_{Cap} + 4J_{PCap}] W_{Cap} + [J_{AGate} L_{Gate} + J_{PGate}] W_{Gate}} \qquad (4.20)$$

The ratio of W_{Gate} to W_{Cap} can be defined as:

$$K_{CG} = \frac{W_{Gate}}{W_{Cap}} \tag{4.21}$$

In a sensible DRAM cell design, K_{CG} should lie between 0.5 and 1 (Section 4.4). Using (4.21) to replace W_{Gate} in (4.20):

$$\tau_{SCell} \cong \frac{\rho_{Cap} W_{Cap}\left(1 - \frac{1}{e}\right)}{J_{ACap} W_{Cap} + 4J_{PCap} + J_{AGate} L_{Gate} K_{CG} + J_{PGate} K_{CG}} \tag{4.22}$$

In the special case of $K_{CG} = 1$ (i.e., $W_{Gate} = W_{Cap}$):

$$\tau_{SCell} \cong \frac{\rho_{Cap} W_{Cap}\left(1 - \frac{1}{e}\right)}{J_{ACap} W_{Cap} + 4J_{PCap} + J_{AGate} L_{Gate} + J_{PGate}} \tag{4.23}$$

As in Section 2.3.2, the limiting cases of (4.22) and (4.23) can provide insight into storage time scaling behavior. Not surprisingly, the largest DRAM cells will show the longest storage times, and the upper limit on τ_S as W_{Cap} approaches infinity is determined by the bulk capacitor leakage:

$$\tau_{SCell}(max) \cong \frac{\rho_{Cap}\left(1 - \frac{1}{e}\right)}{J_{ACap}} = \tau_{SCap} \tag{4.24}$$

As W_{Cap} shrinks, the last three terms of the denominator of (4.23) and (4.24) will grow increasingly important to hurt DRAM cell storage time as cell sizes shrink. If L_{Gate} and K_{CG} are fixed as all other device dimensions are shrunk proportionally, maintaining $W_{Cap} = L_{Cap} = W_{Gate}/K_{CG}$, the last three denominator terms of (4.22) and (4.23) do not change. Under these circumstances τ_{SCell} in (4.22) and (4.23) will at worst shrink one-to-one with shrinking W_{Cap}.

In a complete DRAM, the charge that an individual cell must hold is determined by the organization and operational circuit requirements of

each chip. However, the storage of 1 million electrons generally represents a reasonable benchmark. With a 0 V to 0.5 V logic swing, a 10 x 10 μm^2 MESFET DRAM capacitor (profile in Figure 4.9) stores 1.25 million electrons. Thus given the device cross-section of Figure 4.9, the 10 x 10 μm^2 capacitor appears to represent a practically-sized MESFET DRAM cell.

Unfortunately, the smallest complete DRAM cell that was directly measured in the course of this work was about 10 times larger. The layout of the cell is pictured in Figure 4.18. Figure 4.19 shows the write pulse train taken from an L_{Gate} = 1 μm $(NH_4)_2S$-treated gate MESFET version of this DRAM cell, while Figure 4.20 shows the complete recovery transient of the cell following the writing of a logic one. The 1/e storage time of this device is 620 msec at room temperature.

Given the above experimental result, it is reasonable to conclude that a 620 msec storage time is attainable in a $W_{Cap} = L_{Cap} = W_{Gate}$ 110 μm, L_{Gate} = 1 μm version of the cell layout of Figure 4.17. By shrinking the $W_{Cap} = L_{Cap} = W_{Gate}$ dimensions of such a cell to 10 μm while maintaining L_{Gate} = 1 μm, a possible layout for a practical DRAM cell that might be used in a large memory array can be obtained. Under the storage time scaling behavior approximated in (4.23), the resulting $(NH_4)_2S$-treated gate MESFET DRAM cell should have a 1/e storage time no worse than 56 msec.

A 1.75 second storage time was obtained on a JFET-accessed layout similar to Figure 4.18. Arguments parallel to those outlined above suggest that a $W_{Cap} = L_{Cap} = W_{Gate}$ = 10 μm, L_{Gate} = 2 μm JFET DRAM cell like Figure 4.17 should have a room-temperature storage time in excess of 150 msec.

4.4 GaAs DRAM Cell Design

Since the operating characteristics of the individual memory cells seriously impact the overall performance of a DRAM chip, selection of the optimum physical cell configuration is crucial. There are many issues which must be considered when designing a DRAM cell, and many of these

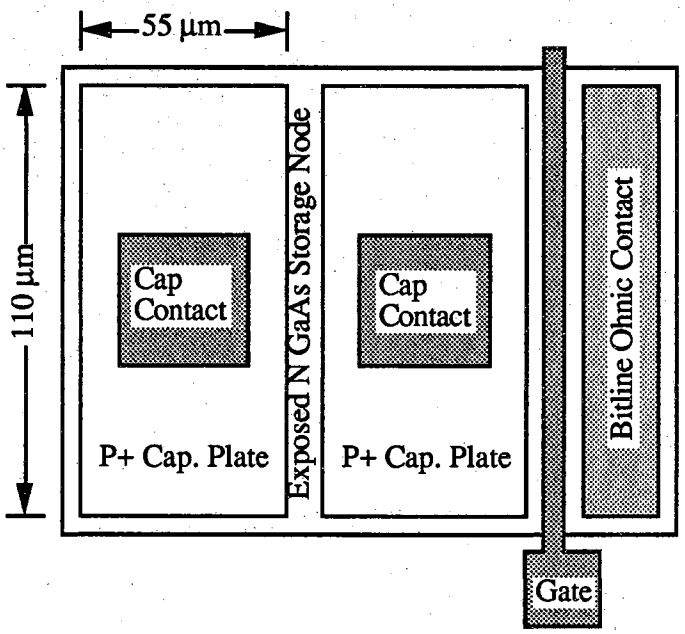


Figure 4.18 Layout of an experimental FET-accessed GaAs DRAM cell. Gate lengths of 2 µm and 1 µm were tested (see text).

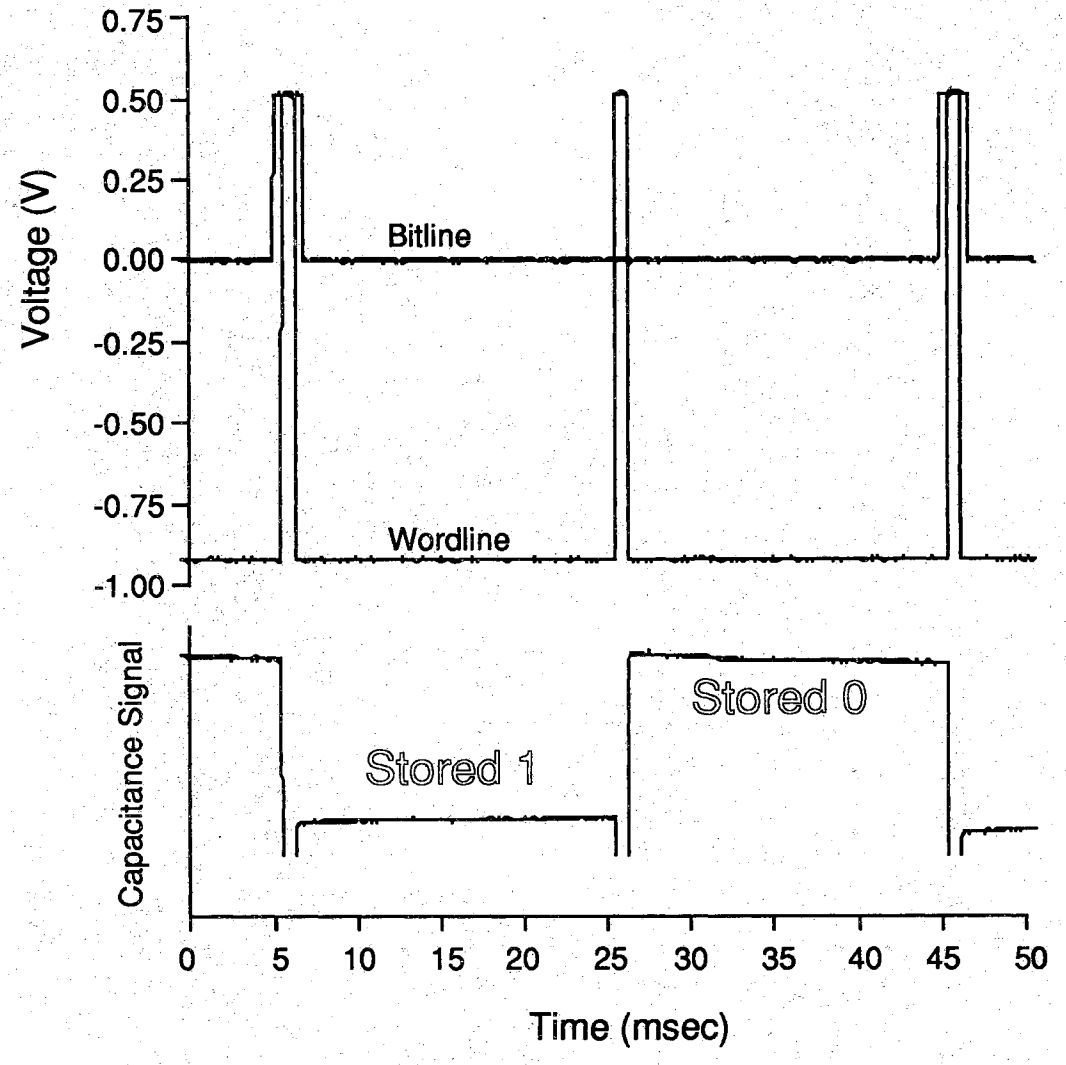


Figure 4.19 Write pulse train taken from an $(NH_4)_2S$-treated gate MESFET DRAM cell with L_{Gate} = 1 μm. The cell layout is given in Figure 4.18, and the capacitance signal shown is averaged.

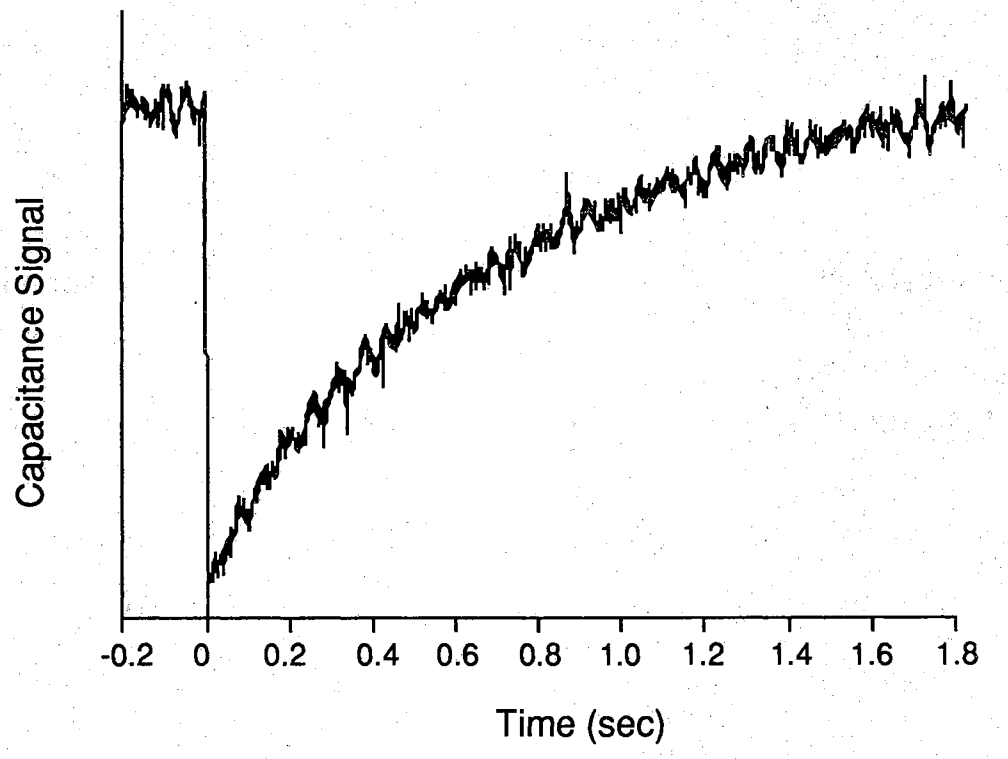


Figure 4.20 Full write one capacitance recovery for the $(NH_4)_2S$-treated gate MESFET DRAM cell with L_{Gate} = 1 μm. The 1/e recovery time is 620 msec. The operating voltages and waveforms used to write the one are shown in Figure 4.19, and the cell layout is shown in Figure 4.18.

have been addressed to a large degree in preceding sections of this work. However, there are several important considerations which have not yet been covered due to the fact that they are specific to certain capacitor-transistor cell combinations. The purpose of this section is to present and evaluate various design trade-offs associated with complete JFET- and MESFET-accessed DRAM cell configurations. Based on the results of this discussion, some cell designs that are compatible with ion-implanted LSI GaAs FET technologies are proposed and evaluated.

4.4.1 Miscellaneous Cell Design Considerations

A high speed RAM chip must consist of high-speed RAM cells. Since DRAM cell read/write operations are based on the movement of charge between the capacitor and the bitline, the fastest cell is one that moves the charge in the shortest time. The most obvious DRAM cell speed consideration is that the turned-on access transistor carry as much current as possible during read/write operations. Transistor currents and speeds have steadily increased with decreasing gate lengths, so an access transistor with a state-of-the-art sub-micron L_{Gate} is naturally desired for use in a high-speed GaAs DRAM. Section 3.3 indicates that subthreshold source-to-drain conduction can be quenched for gate lengths down to a half-micron, so short-channel I_{DS} leakage should not be a factor in DRAM cell storage time until $L_{Gate} < 0.5$ μm devices are considered (provided there is proper optimization of the device channel profile and operating voltages). When transistor leakages do govern cell storage times, one can cut K_{GC} (Figure 4.17 and Relation (4.21)) to gain some storage time. However, this will also cut the current carrying capability of the access transistor to adversely impact cell speed.

To increase FET speed, parasitic capacitances and resistances should be minimized. Parasitic source and drain resistances are minimized in self-aligned structures (like the MESFET structure of Figure 4.9). FET channel-to-substrate capacitances are minimized by insulating material under the channel. In the directly-connected DRAM cell designs of Figures 4.1 and 4.9, the large generation volume in the lightly-doped region

beneath the storage node harms cell storage time. In addition, the large depletion increases the likelihood of soft errors occurring from alpha-particle induced charge [58].

In addition to the current-carrying capability of the access FET, the storage capacitor geometry also impacts the rate at which charge flows within the cell. A difficulty with the JFET cell design of Figure 4.1 is that the doping and thickness of the N layer in the capacitor must be the same as in the transistor channel. Ideally, the doping and thickness of the capacitor's N layer would be much greater than in the transistor channel so that the storage node would not be close to depletion at any logic level. Otherwise, the lateral flow of carriers through the capacitor to the access FET may become restricted and slow the cell's operation as depicted in Figure 4.21.

The above problem is effectively avoided in the MESFET cell of Figure 4.9 because the capacitor N-layer doping-thickness product was chosen large. Even in these devices, a sensible lateral capacitor geometry is advisable if charge is to move rapidly through all lateral portions in the capacitor (i.e., $W_{Cap}/L_{Cap} \sim 1$ in Figure 4.17). Computer simulations suggest that lateral carrier flow within a properly-doped capacitor is sufficient for near- and sub-nanosecond access to the bitline for $L_{Cap} \leq 10$ μm [132].

4.4.2 DRAM Cell Configurations

Perhaps the most popular processes used in the GaAs digital IC industry is the Self-Aligned Gate (SAG) ion-implanted MESFET process [33-36, 39-41]. With the addition of one extra masking step and possible adjustment of transistor implants and threshold voltages (if circuit considerations warranted them), a standard industrial SAG process could produce the DRAM cell of Figure 4.22 [33-36]. The cell storage element is a Schottky junction storage capacitor, which is defined separate from the gate in the final masking step. Unfortunately given the large conventional-gate MESFET leakages that have been documented in this work, any SAG MESFET cell design would most likely suffer from short storage times due

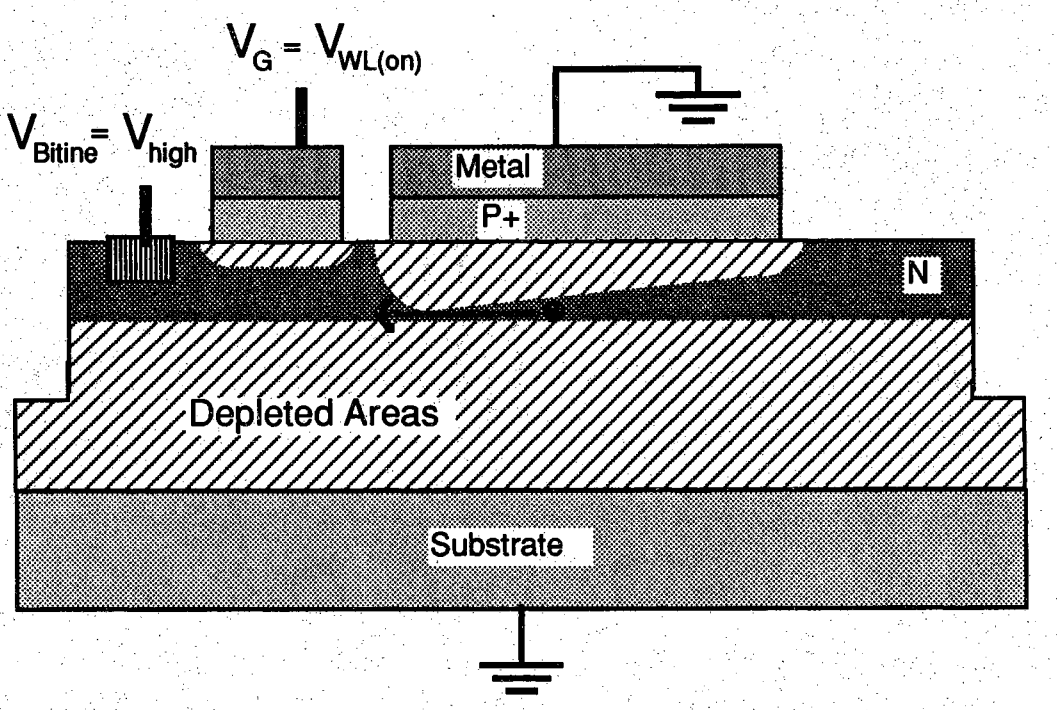


Figure 4.21 Constriction of carriers flowing out of the capacitor during the course of a write one cycle. This phenomenon adversely affects the write speed of the epitaxial JFET-accessed DRAM cell configuration of Figure 4.1.

to Schottky diode leakages. Although the ammonium sulfide treatment of Section 4.2.2 could be employed to produce a low-leakage Schottky capacitor, it is probably not applicable to the gate in a SAG MESFET due to the fact that N^+ source/drains are implanted and annealed at high temperatures following gate definition.

Although the advantages of SAG FET's are lost, a non-self-aligned process could produce DRAM cells with considerably longer storage times. The DRAM cell of Figure 4.23 could be implemented using a standard ion-implanted JFET process [47,51,109]. The deep P implant confines the capacitor junction depletion region so that storage time and alpha-particle noise immunity might be increased. With $(NH_4)_2S$-treated Schottky gate and capacitor junctions, a non-self-aligned version of the MESFET DRAM cell of Figure 4.22 could produce much longer storage times than the its SAG counterpart.

To this point, only directly-connected cells have been considered, but non-directly connected cells are feasible in processes where the addition of a drain ohmic contact doesn't increase the drain-to-substrate leakage (Section 3.2.5.1). This would enable the use of pure dielectric capacitors as DRAM cell storage elements (Figure 2.2a), which in turn would lead to a vast array of FET-capacitor cell combinations. Provided processing and material difficulties could be worked out, variations of 3-D structures being developed for silicon DRAM's might also be applied to GaAs FET-accessed DRAM's (Figure 2.2b, for example).

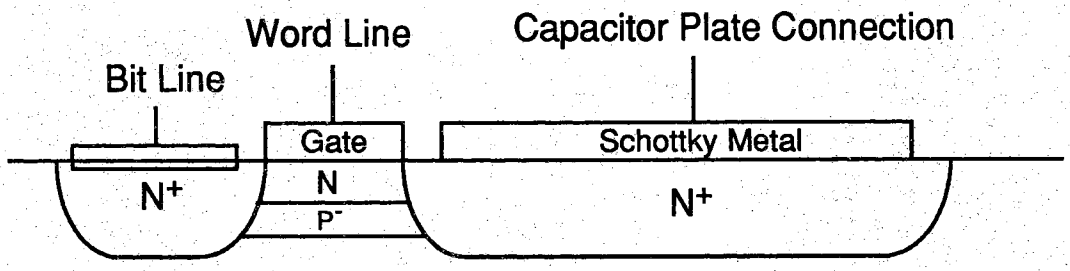


Figure 4.22 A SAG MESFET accessed DRAM cell. With the addition of one masking step, this cell could be produced with commonly-employed GaAs IC processes described in References [33-36] and [39-41].

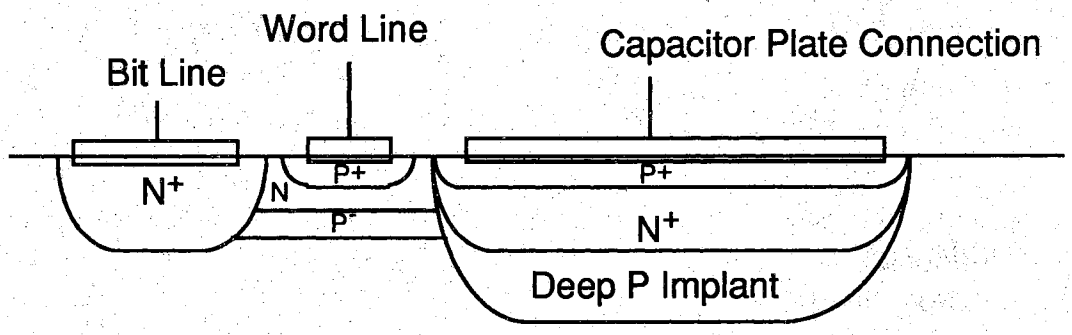


Figure 4.23 An ion-implanted JFET-accessed DRAM cell. This cell could be realized by a variation of the ion implanted GaAs JFET process that has produced a 16K SRAM and a 32-bit RISC microprocessor [47,51,109].

CHAPTER 5 - DEMONSTRATION OF A 2 X 2 DCAM ARRAY

5.0 Introduction

Although isolated FET-accessed cells were presented in Chapter 4, a small array of cells is needed to conclusively demonstrate that GaAs DRAM cells can be individually addressed for reading and writing. To satisfy this requirement, the development of a 2 x 2 bit experimental memory array was undertaken. Instead of an ordinary RAM array however, a content addressable memory (CAM) was built instead.

As outlined in Figure 5.1, a content addressable memory is a RAM array whose data contents can be rapidly searched in parallel. Data can be written to or read from the array just like an ordinary RAM. What distinguishes the CAM from the RAM is the comparison read operation, whereby a keyword is input on the bitlines (columns). If the word stored along a given row matches the keyword input, a word matchline is activated (matchline 2 in Figure 5.1) to denote the row address of the data being sought. This allows a huge time savings over serial searching techniques when trying to locate data items hidden in large unsorted lists.

In addition to RAM capabilities (read/write/store), each CAM cell must be able to compare its current contents with data that is placed on the bitlines to generate the proper matchline output. The matchlines of a given word (row) are tied together in a wired AND configuration, so that all bits in a row must correspond for a word match to occur. In some cases it is advantageous to search for only a few bits in a given word, and this is done by putting a "don't care" state as the keyword in columns that are of no interest (keyword bit 0 of Figure 5.1). In these cases a CAM cell must generate a match condition regardless of it's stored data contents.

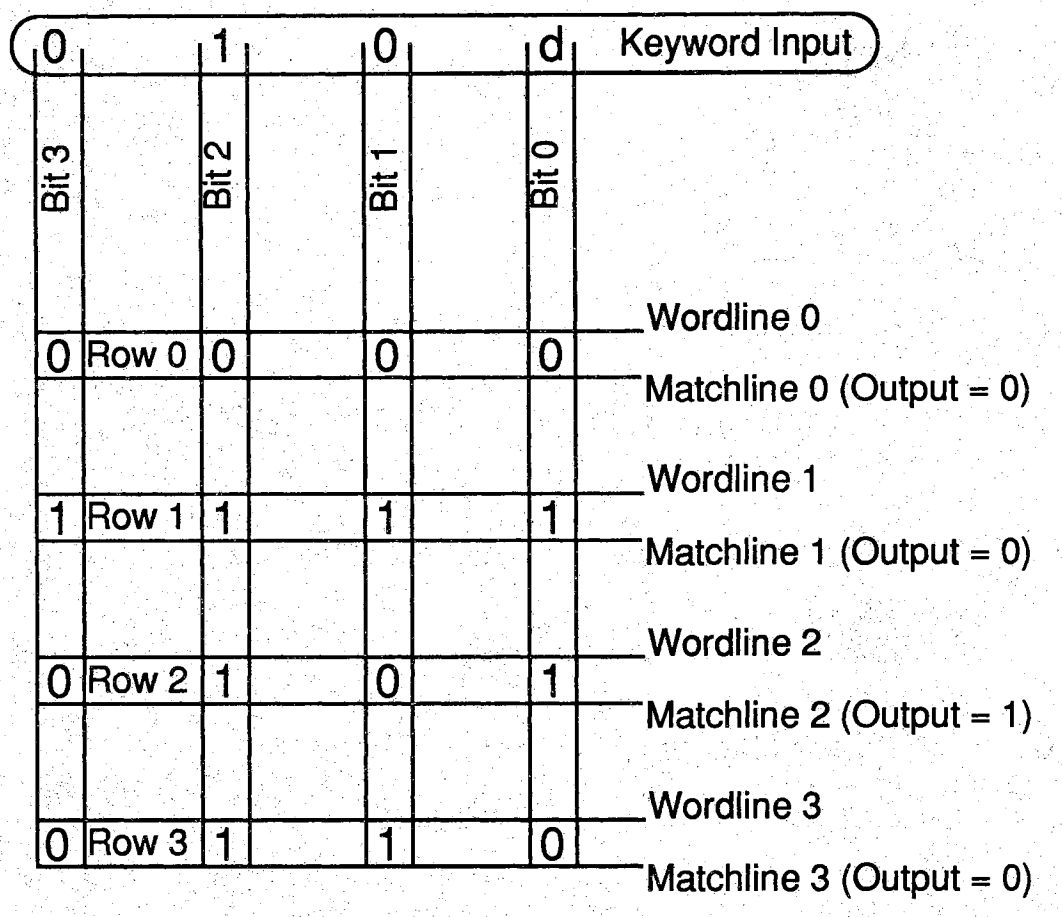


Figure 5.1 Logical function of a content addressable memory (CAM) array. All the stored words in memory are compared simultaneously to the keyword input on the bitlines. The high matchline in row 2 denotes the location of the matching data. In this example only the contents of bits 1-3 matter because bit 0 of the keyword input is a "d" = "don't care".

5.1 The Common N-Channel JFET DCAM Cell

To incorporate one-transistor dynamic RAM technology into a GaAs CAM, the dynamic content addressable memory (DCAM) cell of Figure 5.2 was developed. The cell consists of two 1-transistor DRAM cells (to store the information and its complement) and a four-transistor XNOR gate for comparing the cell contents to keyword data on the bitlines. The DRAM part of the cell is based on the previously proven epitaxial JFET cell of Section 4.1, and was chosen for its reliable simplicity. The process is outlined pictorially in Figure 5.3 and described in detail in the runsheet of Appendix 2. The first five process steps define the JFET's and storage capacitors, while the last two are used for top metal interconnect. The process choice meant all the transistors in the CAM cell were N-channel depletion mode JFET's with $V_{T0} = -1.0$ V.

The read/write/store operation of the DRAM part of the cell is the same as in Section 4.1, and as such, similar DRAM operating voltages ($V_{low} = 0$ V, $V_{high} \approx 1$ V, $V_{WL(off)} = -1.5$ V, and $V_{WL(on)} = 0.5$ V) were chosen. The content matching function can be understood through Figure 5.2 and Table 5.1. Table 5.1 gives the electrical state of the cell for the cases of interest whereby: 1) the bitline input matches the stored contents generating a match output ($V_{Matchline} \approx 2$ V), 2) the bitline input is the opposite of the stored contents generating a no-match output ($V_{Matchline} \approx 1$ V), and 3) the bitline input is a logical "don't care" generating a match output regardless of the stored contents.

Because the DRAM storage nodes are connected to the P^+ gates of XNOR JFET's T1 and T4, the XNOR's must use positively shifted logic levels to prevent discharge of V_{NL} or $V_{NR} = V_{high} \approx 1$ V stored in the DRAM through a forward bias on the XNOR JFET's gate-to-channel PN junction (Figure 5.2). Although this results in a body effect threshold voltage shift away from $V_{T0} = -1.0$ V for the XNOR transistors, the change in FET characteristics is in sufficiently small and in the proper direction ($V_T(V_{SB} = 1.0) = -0.87$ V) that it has little effect on circuit operation.

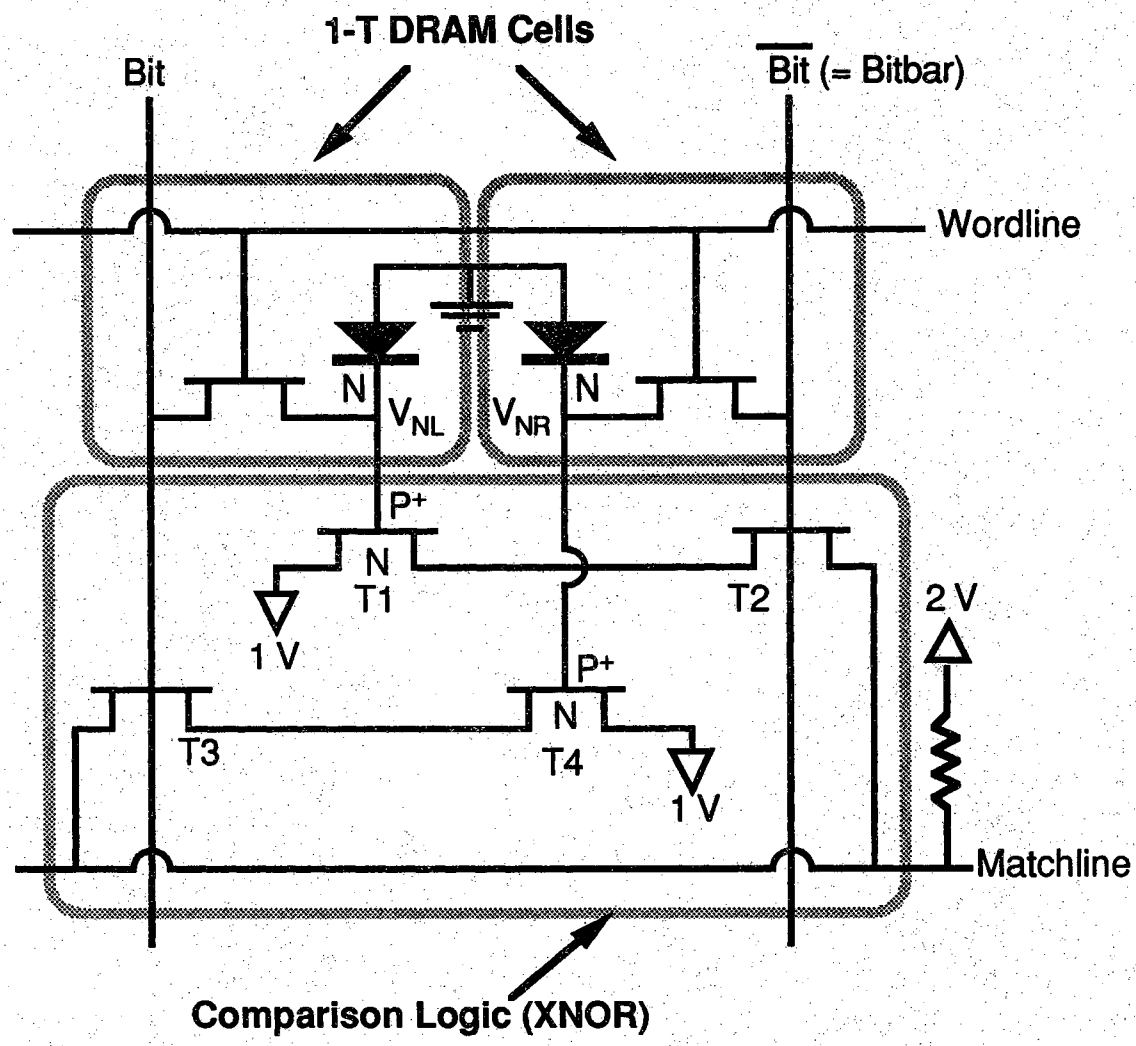
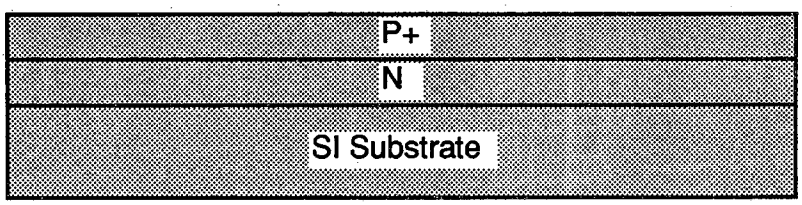
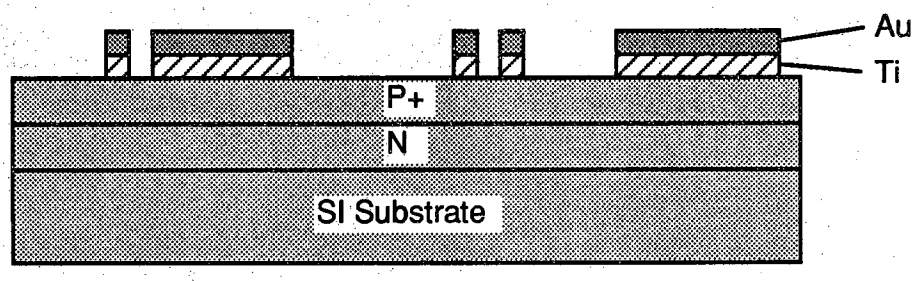


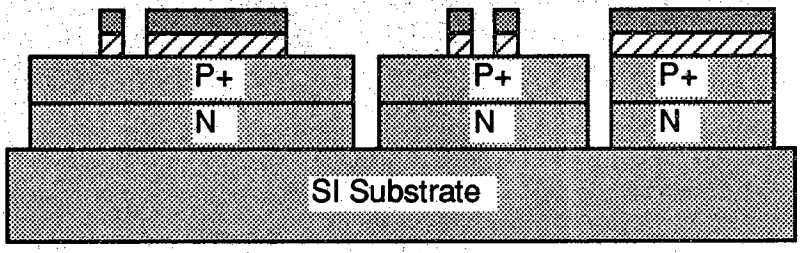
Figure 5.2 JFET GaAs dynamic CAM cell. The data contents are stored in two 1-transistor JFET-accessed GaAs DRAM cells, and comparison operations are performed with the XNOR logic (see text and Table 5.1). All the transistors are depletion-mode epitaxial JFET's with V_{T0} = -1.0 V.



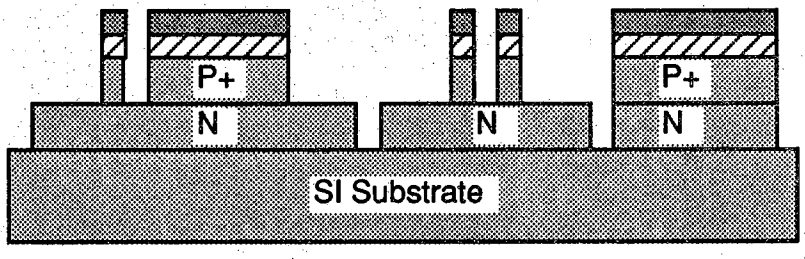
Step 1: Grow Film on Semi-Insulating Substrate.



Step 2: Deposit and Pattern Ti/Au P+ Contacts.

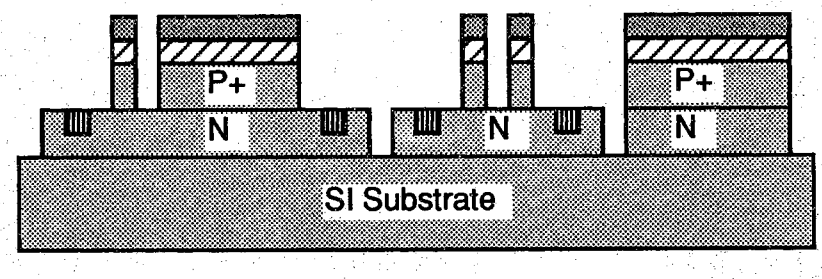


Step 3: Mesa Etch.

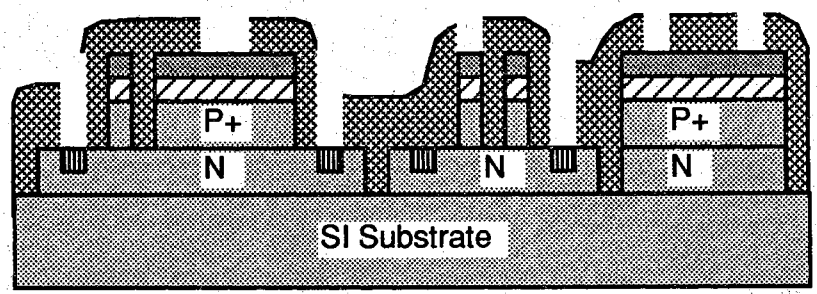


Step 4: Surface Exposure Etch.

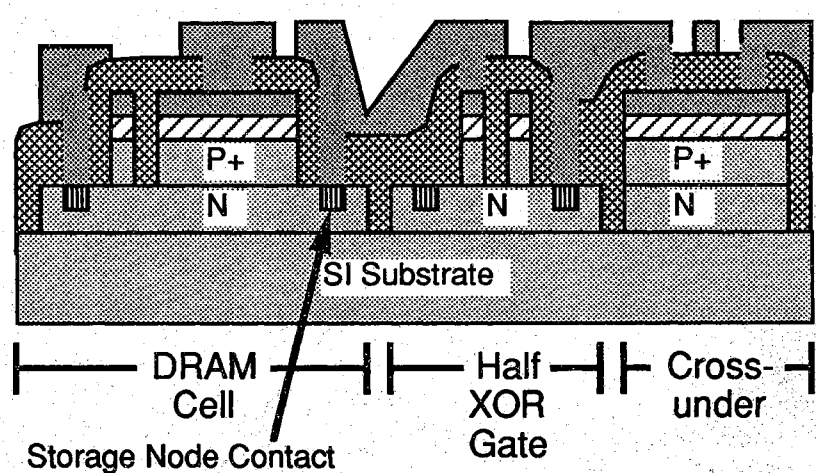
Figure 5.3 Epitaxial JFET DCAM array process sequence.



Step 5: Ohmic Contact Deposition and Alloy.



Step 6: Polyimide Application and Via Etch.



Step 7: Interconnect Metal Deposition.

Figure 5.3, continued

Table 5.1 Electrical truth table demonstrating the operation of the DCAM cell comparison logic circuitry. The voltages given are approximations.

Contents		Keyword		XNOR Transistors				Match
V_{NL} (V)	V_{NR} (V)	V_{Bit} (V)	V_{Bitbar} (V)	T1	T2	T3	T4	$V_{Matchline}$ (V)
0	1	0	1	OFF	ON	OFF	ON	2
0	1	1	0	OFF	OFF	ON	ON	1
0	1	0	0	OFF	OFF	OFF	ON	2
1	0	0	1	ON	ON	OFF	OFF	1
1	0	1	0	ON	OFF	ON	OFF	2
1	0	0	0	ON	OFF	OFF	OFF	2

5.2 Array I/O Circuitry

Because the process did not allow for enhancement-mode devices to use as FET logic drivers, the peripheral circuitry necessary to support a self-contained RAM chip could not be implemented without the use of level-shifting stages and an addtional power supply [42]. Instead these functions were implemented off-chip in the array testing circuitry. Nevertheless, some I/O circuitry had to be incorporated on-chip if full array functionality was to be demonstrated. The control signals required to address, read, write, and match-read each cell in the 2 x 2 array are outlined in this section.

Figure 5.4 shows a simplified schematic that includes the circuitry necessary to drive the array. For clarity the complementary bitlines are not shown because they are driven in the same manner as the bitlines B1 and B2. This allows the representation of the DCAM cells to be simplified to a 1-T DRAM cell plus an XNOR gate. The chip boundary is denoted on the figure by the large fuzzy square, which distinguishes on- and off-chip electronic components. The wordlines (W1 and W2) are purely for input

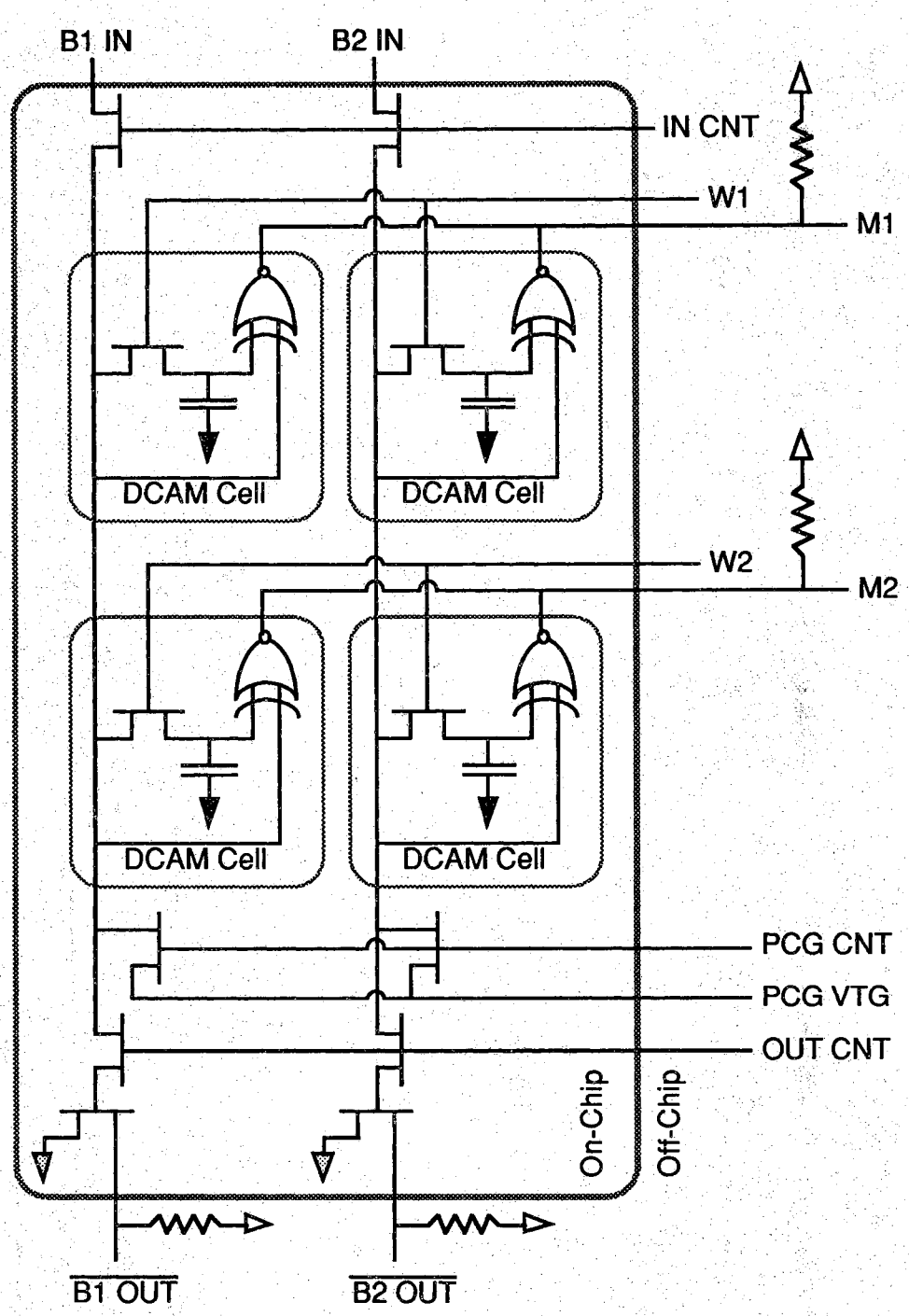


Figure 5.4 Simplified DCAM test chip schematic showing internal and external I/O circuitry.

so they can be connected directly to a test pattern generator. The match lines (M1 and M2) are driven by the CAM cell XOR gates, so their outputs can be completed with external pull-up resistors to a power supply.

The bitlines are more complicated because they must be multifunctional. Pass transistors, which can be gated with the same on and off voltages as the DRAM wordlines, are used to connect and isolate the bitlines to inputs and outputs at the proper time. During a write or match-read operation, the bitlines are externally driven by the pattern generator (connected to inputs B1 IN and B2 IN) through pass transistors controlled by INP CNT. Read operations require precharge and sense cycles. The precharge cycle consists of all bitlines being taken to a predetermined voltage, and this is accomplished by connecting all the bitlines to the voltage input at PCG VTG by turning on pass transistors with a PCG CNT signal. The bitlines are then isolated to a floating condition by turning off the PCG CNT pass transistors. The selected wordline (W1 or W2) is turned on to connect the bitline to the storage capacitor, and the bitline voltage will change as it charge shares with the addressed storage capacitor.

Charge sharing requirements dictate the voltage on the bitlines must be measured using a low-capacitance on-chip detection scheme. Through some pass transistors (controlled by OUT CNT), the bitlines are connected to the gates of output transistors. With the output transistors properly biased to external resistors and power supplies, the change in gate (bitline) voltage will cause the outputs B1 OUT and B2 OUT to register corresponding voltage changes. Proper biasing of the output circuit includes keeping the P^+ gates of the output FET's negative with respect to the N-channel so that bitline charge isn't leaked through a forward-biased P^+N gate-to-channel junction. Thus the logic levels of the output transistors are shifted positive similar to the matchline voltages. The buffered outputs are not subject to charge sharing, so their voltages can be measured directly with an oscilloscope probe.

5.3 Layout and Fabrication

Figure 5.5 depicts the layout of a single DCAM cell. The capacitors were made large to insure the presence of a large bitline signal during reading. The wordline and the matchline run horizontally parallel to each other through the middle of the cell on first level (gate) metal, while the bitlines and voltage supplies run vertically on the top level interconnect. The XNOR V_{SS} line along the left and right cell borders are shared with adjacent CAM cells in the array. For the voltage stored on the capacitor to gate the XNOR (Figure 5.2), an alloy contact to the storage node is needed (Figures 5.3 and 5.5). This contact is kept as small as possible to reduce any storage time degradation that the contact might cause (Section 3.2.5.1).

The mask set was divided into four different chips. The first three chips contained different-sized versions of the 2 x 2 DCAM array. The smaller tolerance arrays were made from scaled (half-sized and quarter-sized) copies of the largest tolerance array. The layout of the largest tolerance 2 x 2 array is shown in Figure 5.6, and the design rules used are evident in Figure 5.5. The array required 19 wire bond pads, which were 100 x 100 μm^2 with 50 μm spacing. The fourth chip, as well as leftover space on the first three chips, contained a wide variety of test structures. These test structures included various sizes and geometries of isolated storage capacitors, MESFET- and JFET-accessed DRAM cells, DCAM cells, and process testers. The devices were fabricated on approximately 1-inch square wafers using the process runsheet of Appendix 2.

5.4 Electrical Characterization

The functional characterization of the DCAM was divided into two major parts. Prior to attempting operation of the entire array, individual DCAM cells and related chip test structures were characterized (Section 5.4.1). Measurements describing the complete 2 x 2 DCAM array functionality are described in Section 5.4.2. All measurements reported in this section were conducted at room temperature.

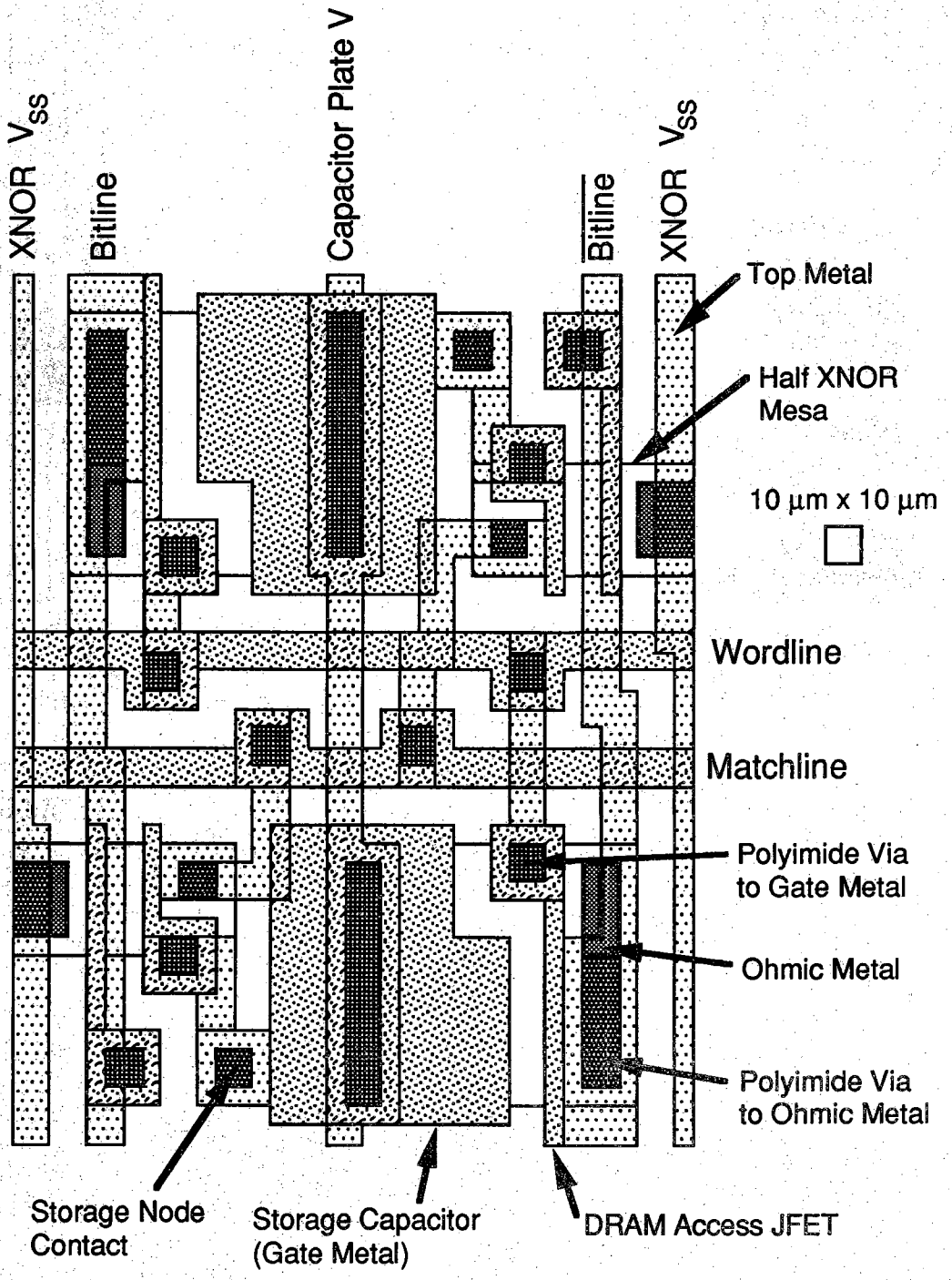


Figure 5.5 Epitaxial GaAs JFET DCAM cell layout.

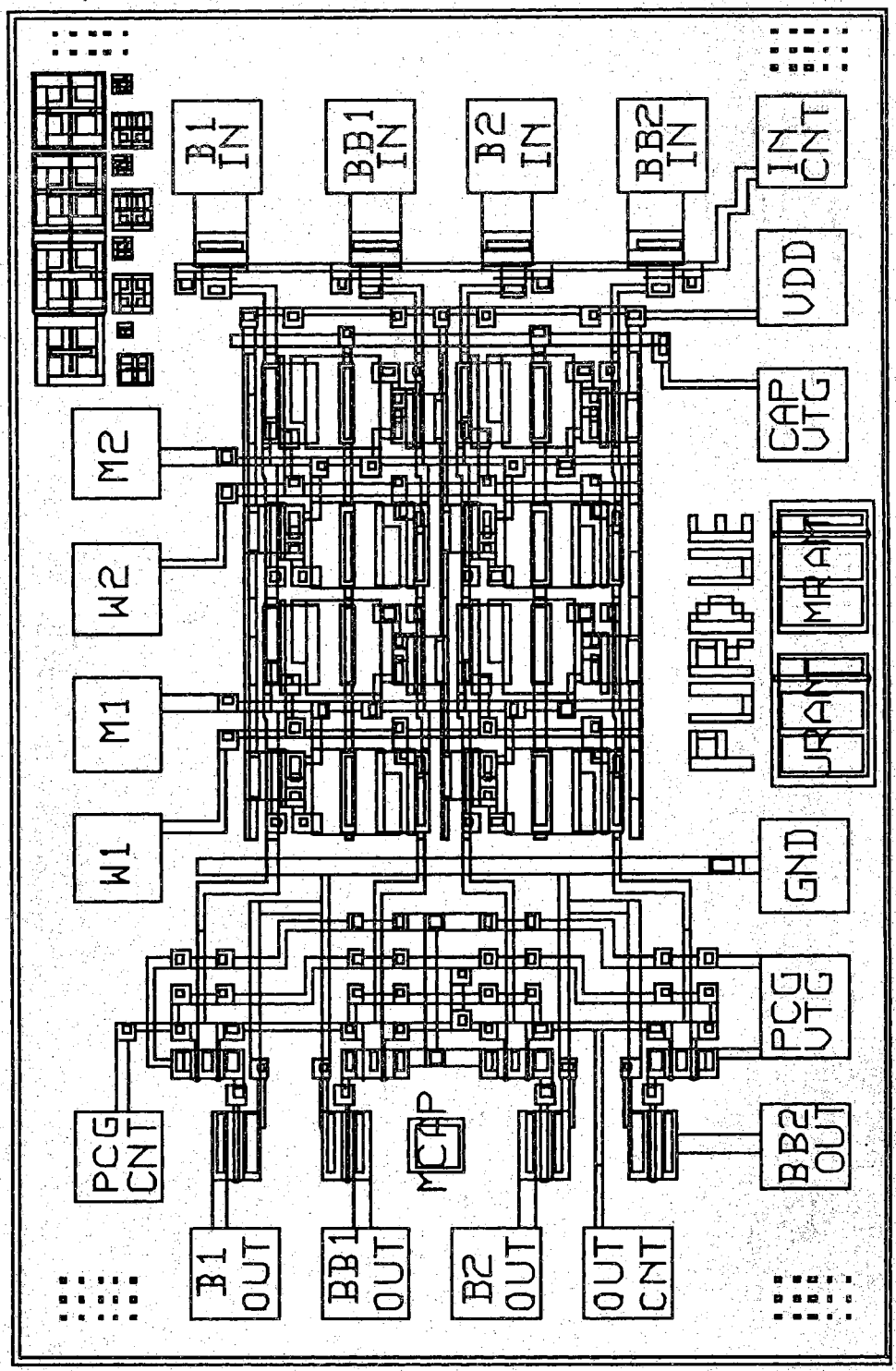


Figure 5.6 Full-size 2 x 2 DCAM array test chip.

5.4.1 DCAM Cell Characterization

Initial characterization was carried out on a dark box probe station prior to wafer die breakup. The proper operation of an individual DCAM cell is demonstrated by the waveforms recorded in Figure 5.7. The cell is initially in a storage state with the DRAM access transistors off ($V_{WL(off)}$ = -1.3 V). A logic zero is written to the cell by taking the bit to V_{low} = 0 V (logic 0) and its complement to V_{high} = 1.0 V (logic 1) with the wordline on ($V_{WL(on)}$ = +0.4 V). The data is kept on the bitlines for one clock cycle longer than the wordline is on to insure that timing skew errors between the falling edges of the bit- and wordlines don't corrupt the data written to the cell. Following an idle storage state cycle, the contents of the cell are compared to data placed on the bitlines. The comparison of the 0 stored in the cell to the 0 placed on the bitlines causes no change in the matchline voltage, while the comparison of the stored 0 to a 1 input on the bitlines pulls the matchline low. The don't care compare always generates a match, so the matchline stays high when both bitlines are low. In a similar manner the same comparisons are repeated following the writing of a logic 1 to the cell, and the matchline responds appropriately.

Both the full-sized and half-sized CAM cells worked, but the quarter-sized array failed due to non-openings in the smallest polyimide vias. The range of clock-speeds that were demonstrated was limited. Although normally the testing apparatus easily handles submicrosecond clock speeds, the non-standard operating voltages required to operate the DCAM limited the test setup speed to a fastest clock period of 10 μsec. The alloy contact to the storage node (Figures 5.2 and 5.5) damaged cell storage time to the point where the array no longer functioned for system clock periods greater than 5 msec. The blame for apparent short τ_S was placed on the alloy contact, since individual DRAM cells with no storage node contacts showed 1 to 2 second storage times.

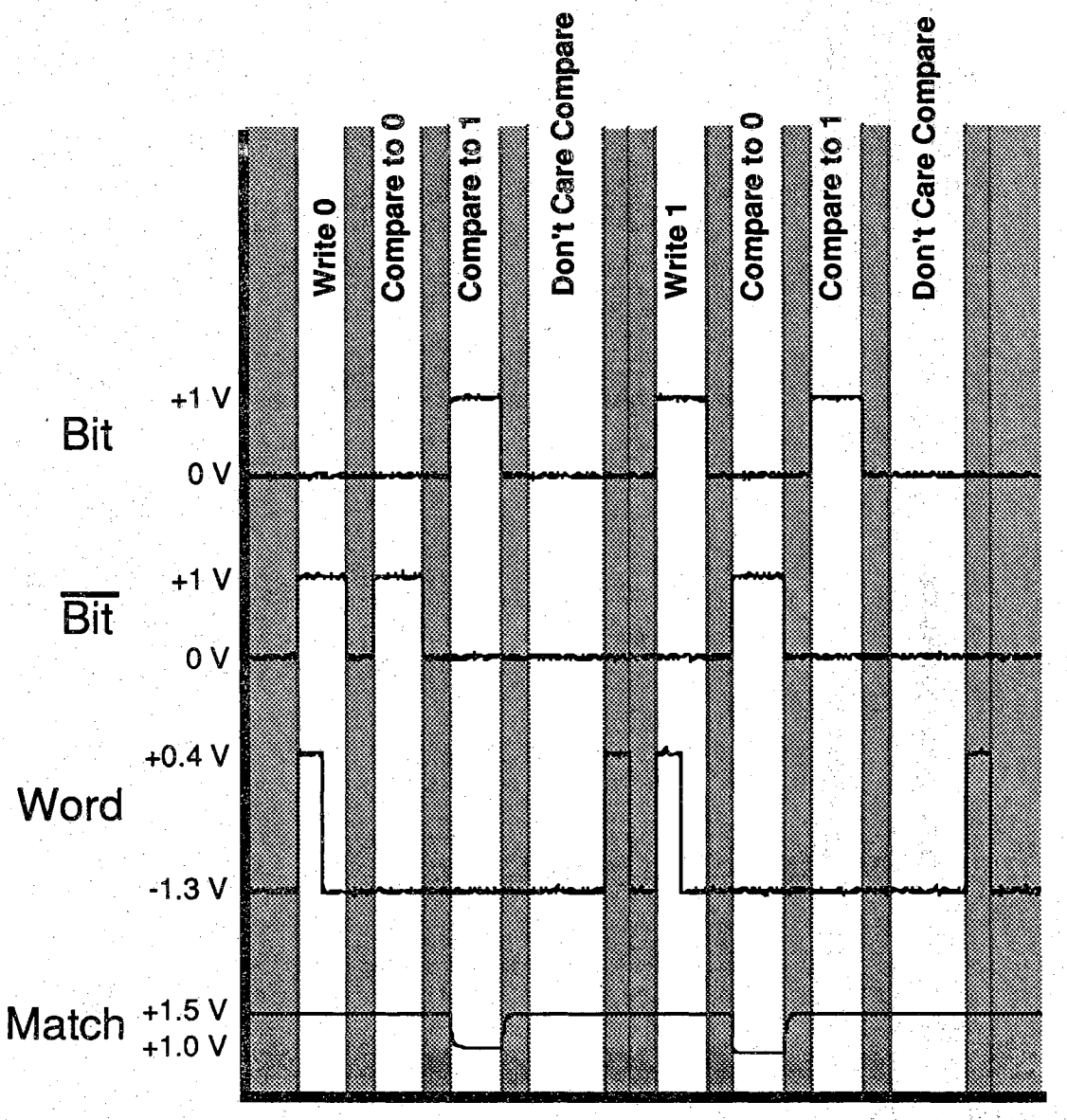


Figure 5.7 Waveforms demonstrating the proper operation of a single GaAs DCAM cell. The system clock period (i.e., the width of the narrowest pulse) is 1 msec.

5.4.2 Functional Demonstration of the 2 x 2 DCAM Array

Following diamond-scribe assisted breakup of the wafer, an individual die containing a full-sized 2 x 2 DCAM array was mounted into a 24-pin DIP package and wire bonded for testing. Functional testing of the array was carried out using a Tektronix 9100 Digital Analysis System (DAS), a Test Systems Strategies LFS-2 test stand, and a Tektronix 11401 Digitizing Oscilloscope. The DAS provided the programmable control signals necessary to drive the array, while the test stand provided a custom interface between the DAS and the 24-pin DIP socket. The digitizing oscilloscope recorded input and output waveforms. Control signals were routed from the DAS through the test stand to the 24-pin DIP socket using a wire-wrapped configuration board. The wiring custom-built for testing the DCAM array provided slots for measuring and supplying voltages, and included adjustable output pull-up resistors. The control signal pattern (i.e., 1's and 0's) is set by programming the DAS, but the operating voltages seen by the chip are set by external DC supplies which power various output busses on the test stand.

The functional characterization of the DCAM array was divided into two parts. The first concern was to verify the proper operation of the GaAs DRAM array by writing, storing, and reading-back various test patterns. This is demonstrated by the measured waveforms of Figures 5.8 and 5.9. In order to understand these waveforms, it is useful to recognize that the 2 x 2 DCAM array is now being operated as a 4 x 4 DRAM array, with both input and output accomplished via the bitlines. Figure 5.8 is a blown-up portion of Figure 5.9 that details the write-store-read test on the 4-bit input combination of all 0's. The captions along the top of the Figure 4.8 timing diagram annotate each step in the sequence. The control signals PCG CNT, IN CNT, and OUT CNT were used as described in Section 5.2. The test sequence starts by writing all 4 bits of memory, a 0 0 for the two bits in row W1 followed by another 0 0 for the two bits in row W2. Usually the precharge voltage is halfway between DRAM V_{high} and V_{low}, but to save on the number of power supplies needed for testing it was set to V_{high}. The successful read-back of the stored data can be witnessed by the response of the bitline OUT signals when the appropriate wordline goes

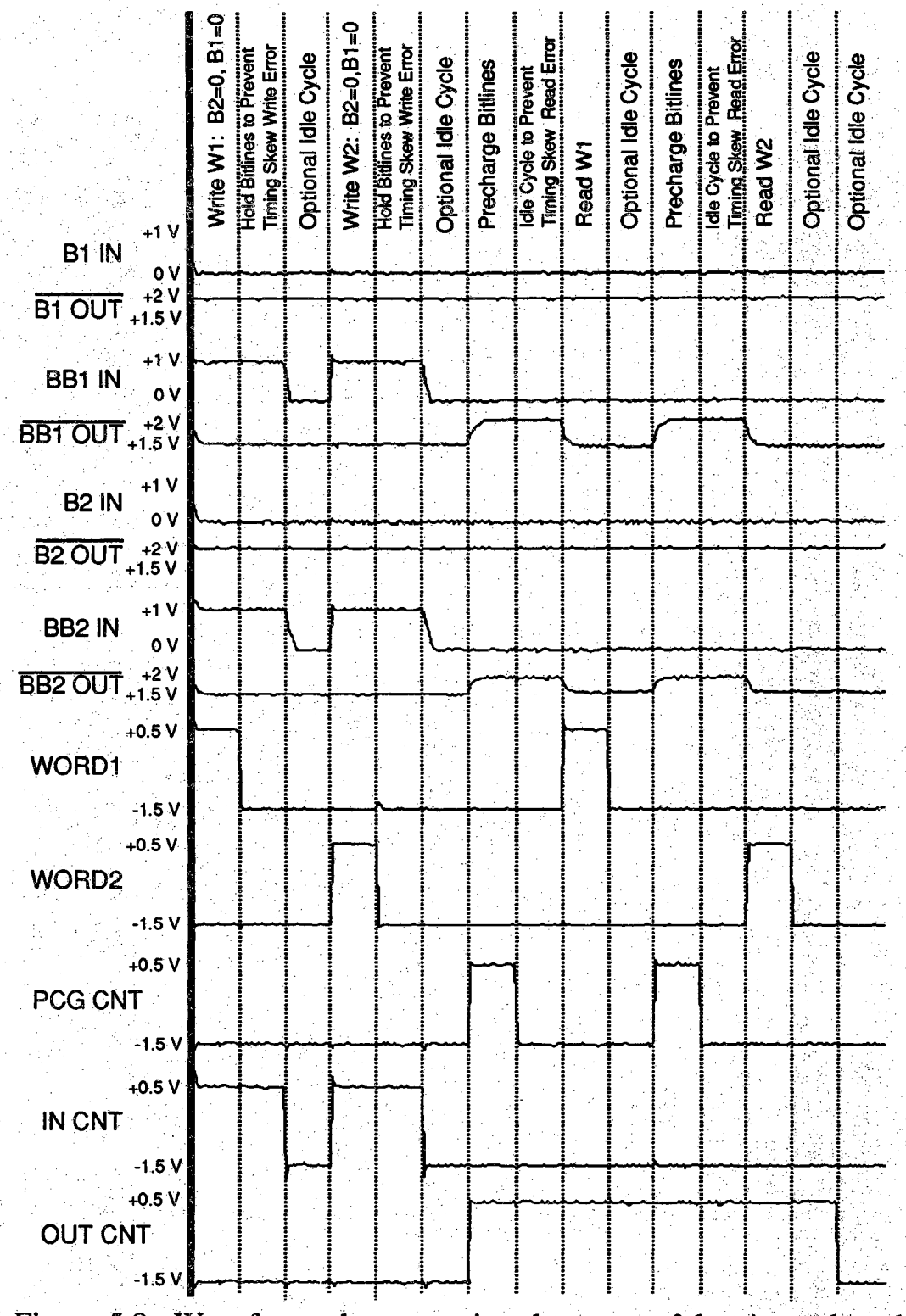


Figure 5.8 Waveforms demonstrating the successful write and read of a 4-bit pattern of all zeros. Clock period = 100 μsec.

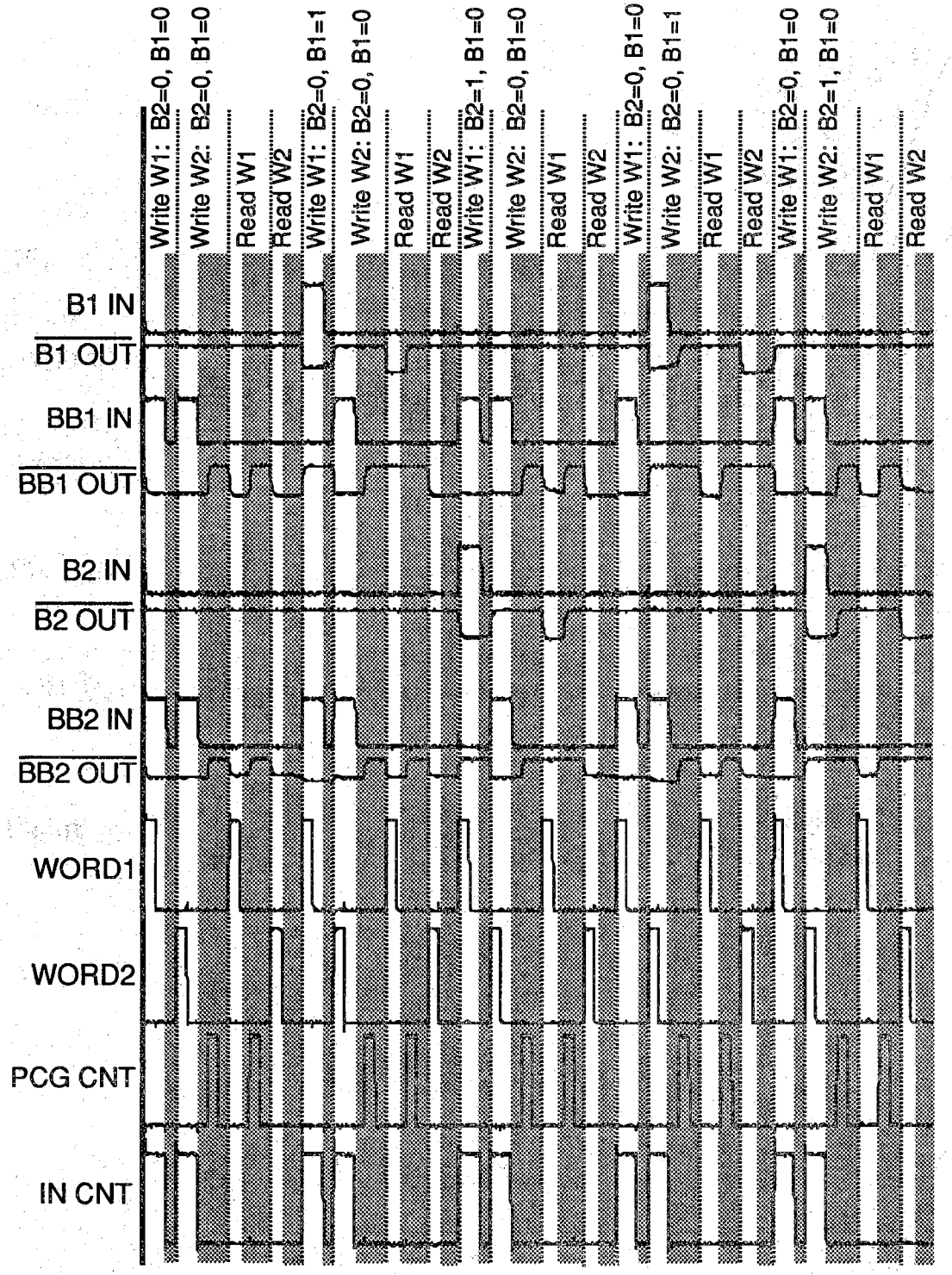


Figure 5.9 Waveforms demonstrating successful write and read operation of DCAM array for 5 input combinations. Clock = 100 μsec.

high. This test sequence is repeated for various 4-bit test patterns in Figure 5.9, and the array successfully passed all DRAM read/write test patterns. The unsharpness of the rising and falling edges of the waveforms is due to shortfalls in the testing setup, and does not reflect speed limitations in the array.

With proper data storage demonstrated, waveforms verifying the match read capability of the DCAM array are shown in Figure 5.10. In a two-bit word where each digit could be a 0, 1, or d = "don't care", there are nine possible combinations that could be input as the keyword on the bitlines. These are shown in columns B1 and B2 in the truth tables across the top, and form a basis for performing 9 comparison read tests for each 4-bit data pattern that's stored in the array. The test sequence of Figure 5.10 consists of writing a 4-bit pattern into the array (shown along the figure bottom), and then performing all 9 possible comparison read operations against the stored data. The truth tables across the figure top show the correct matchline outputs M1 & M2 for each keyword input when compared against the six different stored data combinations shown along the figure bottom. An inspection of the matchline and bitline waveforms reveals that the DCAM array functions correctly for all 54 combinations tested in Figure 5.10.

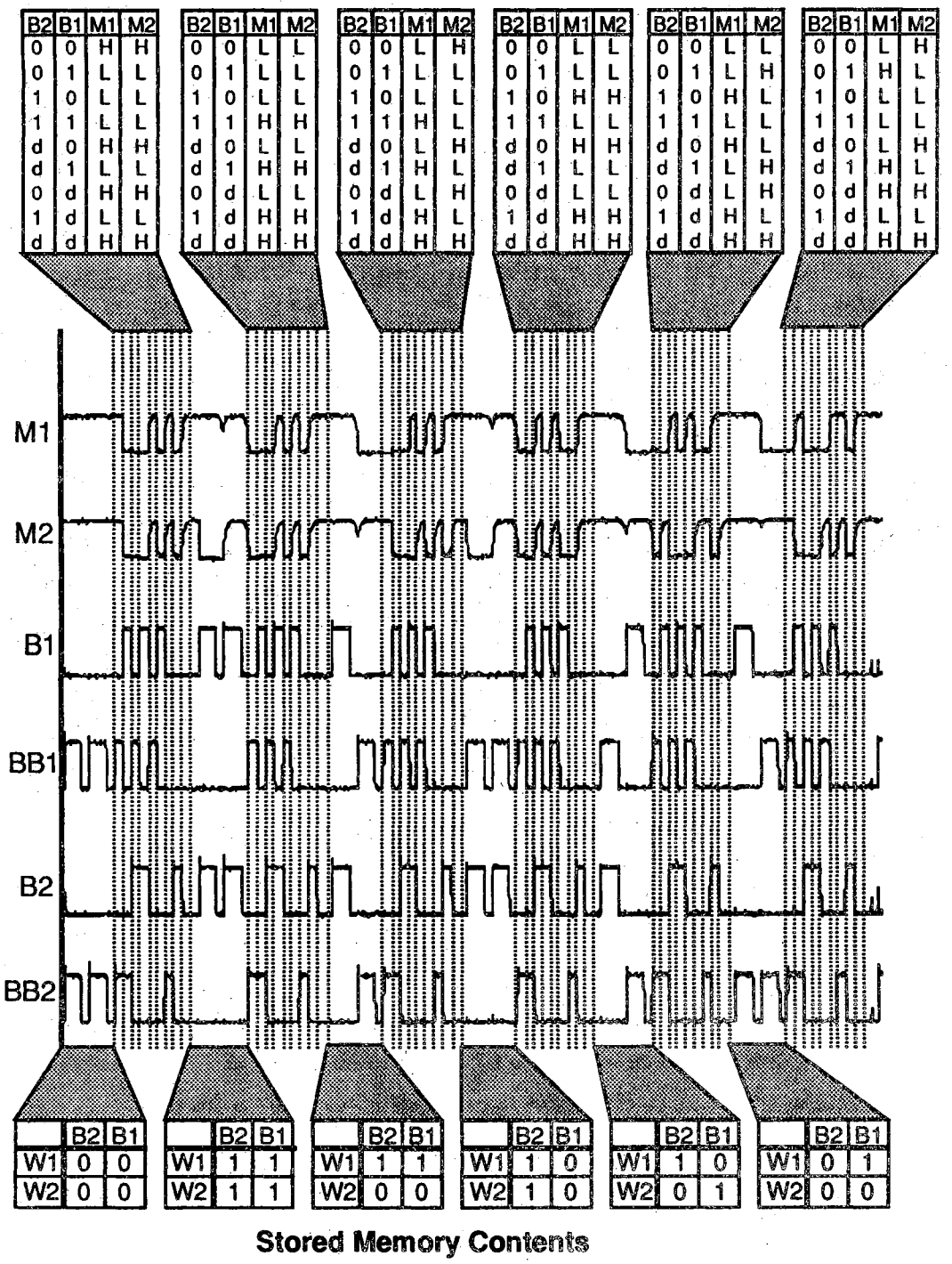


Figure 5.10 Waveforms verifying successful content addressable memory operation. Clock = 100 μsec.

CHAPTER 6 - RECOMMENDATIONS FOR FURTHER RESEARCH AND CONCLUSION

6.0 Recommendations For Further Research

Though many important issues have been addressed throughout the course of this research, some unanswered questions remain. Perhaps the most important questions pertain to the functional manufacturability and speed of large GaAs DRAM arrays; however, these issues probably lie beyond the realm of university research and should instead be investigated in a corporate production environment. There are nevertheless some device-level issues that could be researched at the university level, and these are outlined below.

6.0.1 The Surface Exposure Effect

The experimental results on the surface-exposure effect of Section 2.9 were at best preliminary. Aside from documenting the existence of the effect, the results did not give a clear indication of the physical mechanisms responsible for the reduced storage times in surface-exposed devices. A more detailed theoretical and experimental study of this phenomenon is needed. The study should focus on the storage time as function of device geometry, with the explicit purpose of identifying the limiting mechanism as either surface generation, surface diffusion, a combination of the two, or an as yet unidentified third parasitic leakage mechanism. If surface generation is thought to play a significant role, the As_2S_3 glass treatment of Section 2.10 might passivate the surface-exposed areas to significantly increase device storage times.

6.0.2 Schottky Diode Storage Capacitors

Although the theoretical possibility of Schottky diode charge storage capacitors was introduced in Section 2.14 from data measured as part of another project, no experimental capacitor devices were fabricated or characterized. An experimental study of Schottky-N-P capacitors is needed to check the validity of the theoretical calculations presented. The storage time performance of more heavily-doped capacitors with high charge storage densities must be documented. If sufficient charge storage is demonstrated, a completely metal-semiconductor FET accessed DRAM cell similar to Figure 4.22 could be constructed.

6.0.3 Arsenic Sulfide Glass Treatment to Reduce Edge Generation

The results of initial experiments on the As_2S_3 glass to reduce surface generation are promising. Unfortunately Figure 2.45 represents the sum of data collected on the treatment in reverse bias; more data on a wider variety of P/A ratios is needed to assimilate the true reduction in surface generation current. An attempt to collect such data on PN junction diodes (c.f. Figure 2.28) failed due to the series resistance of the As_2S_3 treatment. Any future studies should therefore be conducted on PNP capacitors, whose storage times are less susceptible to parasitic series surface resistances.

6.0.4 Experimental Verification of Ultra Small DRAM Cells

To facilitate capacitive measurements, the experimental DRAM cells presented in this work were all much larger than would be used in an actual memory chip. Though scaling dependencies dictate that acceptable storage times can be obtained in realistically-sized DRAM cells, an actual demonstration of a small cell could prove useful. Such measurements could be accomplished by having the bitline connection directly gate a

nearby FET on the chip, similar to what was done for the bitline outputs in the DCAM array in Chapter 5.

6.0.5 Electrical Measurement of Cell Speed

Because the technology was developed for high-speed operation, it would be useful to experimentally demonstrate the read/write access speed of these cells. An effort was made toward that end in Chapter 4, but measurement equipment limitations prevented testing below 20 nS. Given careful use of the proper equipment, it might be possible to actually measure the speed of the DRAM cell, which computer simulations suggest are in the range of a nanosecond or less.

6.1 Research Summary

One-transistor dynamic memories based on GaAs JFET and MESFET technologies have been investigated for use in high-speed applications. The performance of diode junction capacitors have been researched for use as charge-storage elements, and their performance appears satisfactory for use in room-temperature DRAM's. Charge densities in excess of 2 fC/μm^2 at 1 V logic swing have been obtained, and this is comparable to charge densities obtained in planar silicon DRAM capacitors under 5 V logic swings [133]. 1/e storage times up to 30 minutes at room temperature have been observed in isolated PN junction storage capacitors. The perimeter-to-area dependance indicates that these capacitors could be scaled to minimum dimensions while maintaining adequate storage times for above room-temperature operation.

JFET's and MESFET's have been thoroughly evaluated for use as DRAM access transistors. Through careful device design, process optimization, and proper choice of operating voltages, both transistors appear suitable for use down to gate lengths of 0.5 μm. Direct relationships between logic swing and access transistor threshold voltage

have been derived, and various other DRAM operating circuit considerations have been considered.

The first complete one-transistor dynamic RAM cells in GaAs have been fabricated and characterized. MESFET- and JFET-accessed DRAM cells have shown full read/write capability as well as storage times sufficient for room-temperature operation. These non-optimized cells consume more than two orders of magnitude less power than the best commercial GaAs SRAM cells. A 2 x 2 bit content addressable memory array was built and successfully operated as a demonstration vehicle of the JFET-accessed DRAM cell technology.

6.2 Conclusion

The work outlined here and in Reference [1] has laid the groundwork for the development of a GaAs DRAM technology. Aside from the basic device physics and single-cell research mentioned above, the technology is at a stage where further development needs the extensive resources of industry to start building reasonable-sized arrays. Until digital GaAs gains a more profitable share of the high-speed computing market, however, most companies will hesitate to spend development money an unproven GaAs technology like the DRAM. The future of the GaAs DRAM clearly rests on the ever-evolving role of high-speed GaAs in the ever-evolving marketplace for digital IC's.

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Appendix 1 - Epitaxial MESFET DRAM Cell Runsheet

Steps 1-8 are performed by the MBE staff.

1. Obtain (100) Semi-Insulating GaAs Substrate.
2. Prepare and Load Wafer Wafer for Epitaxial Growth.
3. MBE Grow 1 to 2 μm unintentionally doped GaAs.
4. MBE Grow 500Å P (Beryllium) Doped GaAs (1.0×10^{17} cm^{-3}).
5. MBE Grow 1500Å N (Silicon) Doped GaAs (4.0×10^{17} cm^{-3}).
6. MBE Grow 1000 Å N^+ (Silicon) Doped GaAs ($2.0 \times 10^{18}/cm^3$).
7. MBE Grow 300 Å unintentionally doped GaAs.
8. MBE Grow 700Å P^+ (Beryllium) Doped GaAs (1.0×10^{19} cm^{-3}).
9. Apply Photoresist.
   1. Pre-bake Wafer at 120° C for 10 to 15 minutes.
   2. Allow wafer to cool for 5 minutes.
   3. Spin Shipely AZ 1350 J-SF Resist for 30 seconds at 4400 RPM.
   4. Bake at 90° C for 12 minutes.
10. Align and Expose Surface Exposure Mask.
    1. Karl Suss Mask Aligner, High Precision Alignment Mode with contact pressure set to -0.6 bar.
    2. Exposure time: 6.5 seconds.
11. Develop Photoresist.
    1. 1 AZ 351 Developer : 5 DI.
    2. Develop for approximately 30 seconds until clearfields visible.
    3. Rinse in DI for 60 seconds, Blow Dry with N_2.
    4. Inspect pattern.

12. Surface Exposure Etch.
    1. Prepare 3 H_3PO_4 : 1 H_2O_2 : 100 H_2O etchant solution.
    2. Etch for 2 minutes 15 seconds to remove 1250Å of GaAs. (Etch rate of ~500Å per minute.)

13. Strip Photoresist.
    1. Two 30-second rinses in ACE.
    2. Thorough DI rinse, Blow dry with N_2.

14. Inspect Surface Exposure Etch.
    1. Optical microscope inspection.
    2. Mesure etched depth with Tencor Alphastep.

15. Apply Photoresist.
    1. Pre-bake Wafer at 120° C for 10 to 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Spin Shipely AZ 1350 J-SF Resist for 30 seconds at 4400 RPM.
    4. Bake at 90° C for 12 minutes.

16. Align and Expose Mesa Mask.
    1. Karl Suss Mask Aligner, High Precision Alignment Mode with contact pressure set to -0.6 bar.
    2. Exposure time: 6.5 seconds.

17. Develop Photoresist.
    1. 1 AZ 351 Developer : 5 DI.
    2. Develop for approximately 30 seconds until clearfields visible.
    3. Rinse in DI for 60 seconds, Blow Dry with N_2.
    4. Inspect pattern.

18. Mesa Etch.
    1. Prepare 3 H_3PO_4 : 1 H_2O_2 : 50 H_2O etchant solution.
    2. Etch for 2 minutes 30 seconds to remove 2500Å of GaAs. (Etch rate of 1000Å per minute.)

19. Strip Photoresist.
    1. Two 30-second rinses in ACE.
    2. Thorough DI rinse, Blow dry with N_2.

20. Inspect Mesa Etch.
    1. Optical microscope inspection.
    2. Mesure etched depth with Tencor Alphastep.

21. Wafer Clean
    1. 5 minutes in ACE, TCA, Methanol, and ACE
    2. Thorough DI Rinse, N_2 blow dry.

22. Apply Photoresist.
    1. Pre-bake Wafer at 120°C for 10 to 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Spin Shipely AZ 1350J-SF Resist for 25 seconds at 4400 RPM.
    4. Bake at precisely 84°C for 10 minutes.

23. Align and Expose N-type Alloy Contact Mask.
    1. Karl Suss Mask Aligner, High Precision Alignment Mode with contact pressure set to -0.6 bar.
    2. Exposure time: 7.5 seconds.

24. Develop Photoresist - To be carried out in a fume hood!
    1. Soak in Chlorobenzene for exactly 17 minutes.
    2. Mix 1 AZ 351 Developer : 5 DI solution.
    3. At conclusion of Chlorobenzene soak, carefully (Chlorobenzene is a dangerous carcinogen!) blow dry with N_2.
    4. Develop for approximately 30 seconds until clearfields visible.
    5. Rinse in DI for 60 seconds, Blow dry with N_2.
    6. Inspect pattern.

25. Native Oxide Removal Dip.
    1. Mix 1 NH_4OH : 40 H_2O oxide etch solution.
    2. Etch for 30 seconds to remove native oxide.
    3. DI rinse for 60 seconds, thorough N_2 blow dry.
    4. Place wafer into E-Beam evaporator immediately to minimize re-formation of native oxide on exposed GaAs surface.

26. Evaporate Au-Ge-Ni-Ti Source/Drain Contacts in Varian E-Beam evaporator.
    1. Pumpdown to 1.0 X 10^{-7} torr.
    2. 36 Å Ni = 188 Hz. Beam current: 0.15 A
    3. 125 Å Ge = 391 Hz. Beam current: 0.2 A
    4. 250 Å Au = 2837 Hz. Beam current: 0.1 A
    5. 125 Å Ge = 392 Hz. Beam current: 0.2 A
    6. 250 Å Au = 2838 Hz. Beam current: 0.1 A
    7. 50 Å Ni = 261 Hz. Beam current: 0.15 A
    8. 500 Å Ti = 1326 Hz. Beam current: 0.08 A
    9. 700 Å Au = 7947 Hz. Beam current: 0.12 A

27. Liftoff N-type Alloy Contact Metallization.
    Squirt and rinse with ACE until unwanted metalization is removed.

28. Optical Inspection of N-type Alloy Contact Metalization.

29. Alloy Contacts in Marshall Oven for 1 minute at 350°C.

30. Inspection of N-type Contact Alloy.
    1. Optical Inspection for change in Au-Ge-Ni surface morphology.
    2. Electrically probe for ohmic source to drain conduction.
    3. If electrical probe shows inadequate results, repeat anneal at a higher oven temperature.

31. Apply Photoresist.
    1. Pre-bake Wafer at 120°C for 10 to 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Spin AZ 1350J-SF Positive Resist for 25 seconds at 4400 RPM.
    4. Bake at precisely 84°C for 10 minutes.

32. Align and Expose P^+ Contact Mask.
    1. Karl Suss Mask Aligner, High Precision Alignment Mode with contact pressure set to -0.6 bar.
    2. Exposure time: 7.5 seconds.

33. Develop Photoresist - To be carried out in a fume hood!
    1. Soak in Chlorobenzene for exactly 17 minutes.
    2. Mix 1 AZ 351K Developer : 5 DI solution.
    3. At conclusion of Chlorobenzene soak, carefully (Chlorobenzene is a dangerous carcinogen!) blow dry with N_2.
    4. Develop for approximately 30 seconds until clearfields visible.
    5. Rinse in DI for 60 seconds, Blow dry with N_2.
    6. Inspect pattern.

34. Native Oxide Removal Dip.
    1. Mix 1 NH_4OH : 40 H_2O oxide etch solution.
    2. Etch for 30 seconds to remove native oxide.
    3. DI rinse for 60 seconds, thorough N_2 blow dry.
    4. Place wafer into E-Beam evaporator immediately to minimize re-formation of native oxide on exposed GaAs surface.

35. Evaporate Ti-Au P^+ Contacts in Varian E-Beam evaporator.
    1. Pumpdown to 1.0×10^{-7} torr.
    2. 1000 Å Ti = 2651 Hz. Beam current: 0.08 A
    3. 2000 Å Au = 11352 Hz. Beam current: 0.1 A

36. Liftoff Ti-Au P^+ Contact Metallization.
    Squirt and rinse with ACE until unwanted metalization is removed.

37. Optical Inspection of Ti-Au Liftoff.

38. Clean Wafer.
    1. 5 minute soaks in ACE, TCA, Methanol, and ACE.
    2. Rinse thoroughly with DI, Blow dry with N_2.

39. Apply Photoresist.
    1. Pre-bake wafer at greater than 120°C for at least 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Apply 4% PMMA positive E-beam resist.
    4. Spin PMMA for 30 seconds at 4000 RPM.
    5. Bake for 4 hours at 160°C.

40. Direct E-beam write gate pattern.

41. Develop PMMA for gate liftoff.
    1. Develop for 5 to 15 seconds in 3 Cellusolve : 7 Methanol.
    2. Rinse for 60 seconds in Methanol.
    3. N_2 Blow dry.
    4. Inspect Pattern.

Note: Steps 42 and 43 should be performed as rapidly as possible.

42. MESFET Gate Recess Etch.
    1. Prepare 3 H_3PO_4 : 1 H_2O_2 : 100 H_2O etchant solution.
    2. Etch for 1 minute 30 seconds to remove 750Å of GaAs (Ideal etch rate of 500Å per minute.)
    3. Thorough DI rinse.

43. Ammonium Sulfide Surface Treat GaAs
    1. Soak wafer for 2 to 5 minutes in saturated $(NH_4)_2S$ solution This must be done in a Flouroware (NOT GLASS) beaker.
    2. Thorough DI rinse, N_2 blow dry.
    3. Place wafer into NRC themal evaporator immediately to minimize re-formation of native oxide on exposed GaAs surface.

44. Thermally evaporate MESFET gates in NRC.
    1. Do not turn on the ion gage at any time!
    2. Pumpdown for at least 1 hour.
    3. Evaporate aluminum with LN_2 running through substrate holder.
    4. Remove sample from NRC.

45. Liftoff MESFET Gate Metallization.
    1. Squirt with ACE until unwanted metalization is removed.
    2. DI Rinse, N_2 blow dry.

46. Optical Inspection of MESFET Gate Liftoff.

47. Electrical Characterization.

Appendix 2 - Epitaxial JFET 2 X 2 DCAM Array Runsheet

Steps 1-6 are performed by epitaxial growth staff.

1. Obtain (100) Semi-Insulating GaAs Substrate.

2. Prepare and Load Wafer for Epitaxial Growth.

3. Grow buffer layer.
   1 to 2μm unintentionally doped GaAs.

4. Grow sub-channel layer.
   500Å P (Beryllium) Doped GaAs (1.0 X $10^{17}/cm^3$).

5. Grow N-channel layer.
   1300Å N (Silicon) Doped GaAs (4.0 X $10^{17}/cm^3$).

6. Grow P^+ Gate/Cap layer.
   750Å P^+ (Beryllium) Doped GaAs (1.0 X $10^{19}/cm^3$).

7. Mount wafer face down on silicon wafer for backside evaporation.
   1. Pre-bake GaAs and Silicon Wafer at 120°C for 10 to 15 minutes.
   2. Allow wafer to cool for 5 minutes.
   3. Apply Shipley AZ 1350J-SF Positive Resist.
   4. Bake at 89-95 °C for at least 30 minutes.

8. Evaporate 3000Å Au backside contact.

9. Resist Strip.
   Two, 1-minute Acetone rinses.

10. Wafer Solvent Clean.
    1. 5 minute ACE soak.
    2. 5 minute TCA soak.
    3. 5 minute Methanol soak.
    4. 5 minute ACE soak.
    5. DI rinse, N_2 Dry [Note 1].

11. Apply Photoresist.
    1. Pre-bake Wafer at 120°C for 10 to 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Apply Shipley AZ 1350J-SF Positive Resist.
    4. Spin Resist for 30 seconds at 4400 RPM.
    5. Bake at 84°C for exactly 10 minutes.

12. Align and Expose Gate Mask (Darkfield).
    1. Karl Suss Mask Aligner, High Precision Alignment Mode.
    2. Exposure time: 7.5 seconds.

13. Develop Photoresist - To be carried out in a fume hood!
    1. Soak in Chlorobenzene for exactly 17 minutes.
    2. Mix 1 AZ 351 Developer : 5 DI solution.
    3. At conclusion of Chlorobenzene soak, carefully (Chlorobenzene is a dangerous carcinogen!) blow dry with N_2.
    4. Develop for approximately 30 seconds until clearfields visible.
    5. Rinse in DI, Blow dry with N_2.
    6. Inspect pattern.

14. Native Oxide Remval Dip.
    1. Mix 1 NH_4OH : 40 H_2O oxide etch solution.
    2. Etch for 30 seconds to remove native oxide.
    3. DI rinse for 60 seconds, thorough N_2 blow dry.
    4. Place wafer into E-Beam evaporator immediately to minimize re-formation of native oxide on exposed GaAs surface.

15. Evaporate Ti-Au Gates in Varian E-Beam evaporator.
    1. Pumpdown to 1.0×10^{-7} torr.
    2. 1000Å Ti.
    3. 1000Å Au.

16. Liftoff Ti-Au Gate Metallization.
    1. Squirt and rinse with ACE.

17. Optical Inspection of Ti-Au Gate Liftoff.

18. Apply Photoresist.
    1. Pre-bake Wafer at 120°C for 10 to 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Apply Shipley AZ 1350J-SF Positive Resist.
    4. Spin Resist for 30 seconds at 7000 RPM.
    5. Bake at 85 to 90°C for 10 to 15 minutes.

19. Align and Expose Mesa Mask (Lightfield).
    1. Karl Suss Mask Aligner, High Precision Alignment Mode.
    2. Exposure time: 6.5 seconds.

20. Develop Photoresist.
    1. Mix 1 AZ 351 Developer : 5 DI solution.
    2. Develop for approximately 30 seconds until clearfields visible.
    3. Rinse in DI, Blow dry with N_2.
    4. Inspect pattern.

21. Hardbake Resist at 120 °C for 10 to 15 minutes.

22. Mesa Etch.
    1. Prepare 3 H_3PO_4 : 1 H_2O_2 : 100 H_2O etchant solution.
       (Etch rate of 500Å $\bar{=}$ per minute.)
    2. Etch enough to isolate active device areas.
       Remove at least 1800 Å (~ 4 minutes, 30 seconds).

23. Strip Photoresist.
    1. Two 30-second rinses in ACE.
    2. Thorough DI rinse, Blow dry with N_2.

24. Inspect Mesa Etch.
    1. Optical microscope inspection.
    2. Measure etch depth with Tencor Alphastep (Optional).

25. Wafer Solvent Clean (Optional).
    1. 5 minute ACE soak.
    2. 5 minute TCA soak.
    3. 5 minute Methanol soak.
    4. 5 minute ACE soak.
    5. DI rinse, N_2 Dry [Note 1].

26. Surface Exposure Etch.
    1. Fill beaker with DI, cover with aluminum foil, and let stand overnight to stabilize temperature for reproducable etch rate.
    2. Prepare 3 H_3PO_4 : 1 H_2O_2 : 100 H_2O etchant solution.
    3. Etch for ~85 seconds to remove P^+ cap layer (GaAs etch rate of 500Å per minute).

27. Apply Photoresist.
    1. Pre-bake Wafer at 120°C for 10 to 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Apply Shipley AZ 1350J-SF Positive Resist.
    4. Spin Resist for 30 seconds at 4400 RPM.
    5. Bake at 84°C for exactly 10 minutes.

28. Align and Expose Ohmic Mask (Darkfield).
    1. Karl Suss Mask Aligner, High Precision Alignment Mode.
    2. Exposure time: 7.5 seconds.

29. Develop Photoresist - To be carried out in a fume hood!
    1. Soak in Chlorobenzene for exactly 17 minutes.
    2. Mix 1 AZ 351 Developer : 5 DI solution.
    3. At conclusion of Chlorobenzene soak, carefully (Chlorobenzene is a dangerous carcinogen!) blow dry with N_2.
    4. Develop for approximately 30 seconds until clearfields visible.
    5. Rinse in DI, Blow dry with N_2.
    6. Inspect pattern.

30. Native Oxide Remval Dip.
    1. Mix 1 NH_4OH : 40 H_2O oxide etch solution.
    2. Etch for 30 seconds to remove native oxide.

31. Evaporate Ohmic Contacts in Varian E-Beam evaporator.
    1. Pumpdown to 1.0 X 10^{-7} torr.
    2. 36 Å Ni.
    3. 125 Å Ge.
    4. 250 Å Au.
    5. 125 Å Ge.
    6. 250 Å Au.
    7. 50 Å Ni.
    8. 500 Å Ti.
    9. 700 Å Au.

Note: For best results, Steps 32 through 35 should be performed immediately following removal of wafers from the evaporator.

32. Liftoff Ohmic Contact Metallization.
    1. Squirt and rinse with ACE.
    2. DI rinse, N_2 Dry [Note 1].

33. Inspect Metalization.

34. Sinter Contacts in Marshall Oven for 2 minutes at 350°C.

35. Inspection of Ohmic Contact Alloy.
    1. Optical Inspection for change in Ohmic Metal morphology.
    2. Electrically probe for ohmic source to drain conduction.
    3. If electrical probe shows inadequate results, repeat anneal at a higher oven temperature.

36. Wafer Solvent Clean.
    1. 5 minute ACE soak.
    2. 5 minute TCA soak.
    3. 5 minute Methanol soak.
    4. 5 minute ACE soak.
    5. DI rinse, N_2 Dry [Note 1].

37. Apply Polyimide.
    1. Prebake wafer at 120 °C for 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Mix 3 parts DuPont Pyralin 2555 Polyimide with 1 part DuPont T-90XX Thinner.
    3. Spin on thinned Polyimide coating at 7000 RPM for 40 seconds.
    4. Bake precisely at 150 °C for 15 minutes.

38. Apply Photoresist.
    1. If more than 5 minutes has elapsed since completion of Step 37, Pre-bake Wafer at 120°C for 10 to 15 minutes.
    2. Allow wafer to cool for at least 5 minutes.
    3. Apply Shipley AZ 1350J-SF Positive Resist.
    4. Spin Resist for 40 seconds at 7000 RPM.
    5. Bake precisely at 84 °C for 10 minutes.

39. Align and Expose Via Mask (Darkfield).
    1. Karl Suss Mask Aligner, High Precision Alignment Mode.
    2. Exposure time: 7.5 seconds.

40. Develop Photoresist and Polyimide Vias.
    1. Mix 1 AZ 351 Developer : 5 DI solution.
    2. Develop for exactly 60 seconds, after which clearfields should be visible.
    3. Rinse in DI, N_2 dry.
    4. Inspect pattern.

41. Strip Photoresist.
    1. Two 30-second rinses in ACE.
    2. Thorough DI rinse, N_2dry [Note 1].

42. Inspect Polyimide Vias.
    1. Optical microscope inspection.
    2. Measure Polyimide thickness with Tencor Alphastep (Optional).

43. Polyimide Final Cure.
    Bake at 225 °C for 2 hours.

44. Wafer Solvent Clean.
    1. 5 minute ACE soak.
    2. 5 minute TCA soak.
    3. 5 minute Methanol soak.
    4. 5 minute ACE soak.
    5. DI rinse, N_2 Dry [Note 1].

45. Apply Photoresist.
    1. Pre-bake Wafer at 120°C for 10 to 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Apply Shipley AZ 1350J-SF Positive Resist.
    4. Spin Resist for 30 seconds at 4400 RPM.
    5. Bake at 84°C for exactly 10 minutes.

46. Align and Expose Interconnect Mask (Darkfield).
    1. Karl Suss Mask Aligner, High Precision Alignment Mode.
    2. Exposure time: 7.5 seconds.

47. Develop Photoresist - To be carried out in a fume hood!
    1. Soak in Chlorobenzene for exactly 17 minutes.
    2. Mix 1 AZ 351 Developer : 5 DI solution.
    3. At conclusion of Chlorobenzene soak, carefully (Chlorobenzene is a dangerous carcinogen!) blow dry with N_2.
    4. Develop for approximately 30 seconds until clearfields visible.
    5. Rinse in DI, Blow dry with N_2.
    6. Inspect pattern.

48. Evaporate Au Interconnect in Varian E-Beam evaporator.
    1. Pumpdown to 1.0×10^{-7} torr.
    2. 3000Å Au.

49. Liftoff Au Interconnect Metallization.
    1. Squirt and rinse with ACE.

50. Optical Inspection of Au Interconnect Liftoff.

51. Initial Electrical Characterization.

52. Apply Protective Photoresist Layer.
    1. Pre-bake Wafer at 120°C for 10 to 15 minutes.
    2. Allow wafer to cool for 5 minutes.
    3. Apply Shipley AZ 1350J-SF Positive Resist.
    4. Spin Resist for 30 seconds at 4400 RPM.
    5. Bake at 84 to 90 °C for 10 to15 minutes.

53. Separate die using diamond scribe.
    (400 μm die border spacing).

54. Strip Photoresist.
    Two, 1-minute soaks in Acetone.

55. Mount die in 24-Pin DIP package.

56. Wirebond.

57. Functional Electrical Characterization.

[Note 1]: DI rinse implies that the beaker is filled and dumped at least 10 times.

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